

NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Program: B.E

New courses introduced in B.E Electronics and Communication Engineering during the last five years

Name of the Course	Name of the Programme	Weather this course is a new course Introduced during the last five years (Yes/No)	Year of introduction
Radar Engineering	B E Electronics & Communication Engineering	YES	2014-15
Embedded System Software Development	B E Electronics & Communication Engineering	YES	2016-17
IP Networking	B E Electronics & Communication Engineering	YES	2015-16
Analog and Mixed Mode VLSI	B E Electronics & Communication Engineering	YES	2014-15
IOT	B E Electronics & Communication Engineering	Yes	2015-16
Adhoc Wireless Networks	B E Electronics & Communication Engineering	YES	2013-14
ARM Cortex	B E Electronics & Communication Engineering	Yes	2013-14
Automotive Electronics	B E Electronics & Communication Engineering	Yes	2013-14
Artificial Neural Networks	B E Electronics & Communication Engineering	Yes	2016-17
Sensors and Actuators	B E Electronics & Communication Engineering	Yes	2016-17
Random Process	B E Electronics & Communication Engineering	Yes	2016-17
Avionics	B E Electronics & Communication Engineering	Yes	2017-18
Micro Smart Systems	B E Electronics & Communication Engineering	Yes	2018-19
Machine Learning for Pattern Recognition	B E Electronics & Communication Engineering	Yes	2018-19
Software Defined Radio	B E Electronics & Communication Engineering	Yes	2018-19
Advanced Microcontroller	B E Electronics & Communication Engineering	Yes	2016-17


 Signature and Seal
 HoD, ECE
 Head,
 Department of Electronics & Communication Engg
 Nitte Meenakshi Institute of Technology
 Govindapura, Yelahanka
 Bangalore - 560 064

**NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ECE**

1/6/19

The UG and PG BoSPanel Members for the Academic Year 2018-19 held on 25/5/2019 is as given

External Panel Members

Sl. No.	Name	Designation	Member
1.	Dr. N C Shivaprakash	Chief Research Scientist, IISc, Bangalore	VTU Nominee
2.	Dr. H V Ravish Aradhya	Professor, Department of ECE, RVCE	Academic Member
3.	Mr. Praveen B	Principal Engineer Samsung, Bangalore	Industry Member
4.	Mr. Mourya Prashanth	Software Engineer, KPIT, Bangalore	Alumni Member
5.	Mr. Sandeep K	Research Assistant, Raman Research Institute, Bangalore	Alumni Member

Internal Panel Members

Sl. No.	Name	Designation	Domain Expertise
1.	Dr. S. Sandya	Professor and Head, Chairperson, BoS	Embedded System
2.	Prof. N Mahavira Swamy	Professor	Wireless Communication
3.	Dr. S.L. Pinjare	Professor	ASIC Design, Analog and Mixed Mode VLSI
4.	Dr. Raghunandan S	Professor	Multimedia Communication
5.	Dr. H S Prashanth	Professor	Signal and Image Processing
6.	Dr. Rajan K Pandey	Professor	Semiconductor Devices
7.	Prof. Sankar Dasiga	Professor	Embedded System and Automotive Electronics
8.	Prof. Sitaram Yaji	Professor	IP Networking

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9.	Prof. G V C Rajan	Professor, EMERITUS	Space System Engineering
10.	Dr. Rajesh N	Associate Professor	Signal Processing
11.	Dr. Veda S N	Associate Professor	MEMS, Sensors and Actuators
12.	Dr. Manjula B M	Associate Professor	Electronics and Signal Processing
13.	Dr. Madhu Patil	Associate Professor	Digital Communication
14.	Dr. Prasanna G Paga	Associate Professor	Antenna System Design
15.	Dr. Jayavrinda V	Associate Professor	Image Processing and Machine Learning
16.	Dr. Padmavathi N	Assistant Professor	Mathematics

BoS Minutes of Meeting

The Salient Features of BoS Minutes of Meeting held on 25/5/19 is as follows:

1. HOD briefed on the Agenda of BOS meeting.
2. The Agenda was:
 - Discussion on BE 2018-22 Scheme.
 - Discussion on BE 2018-22 Syllabus from 3rd to 4th semester
 - Discussion on BE 2017-21 Scheme.
 - Discussion on BE 2017-21 Syllabus from 5th to 8th semester
 - Discussion on M.Tech VLSI and Embedded Systems Scheme and Syllabus 2018-20
 - Discussion on M.Tech Digital Communication and Networking Scheme and Syllabus 2018-20
3. There was a revision in Scheme and Syllabus of :
 - UG 2018-2021 Scheme and Syllabus, Credits was fixed to 175. With equal distribution of credits across all semesters
 - UG 2017-2021 Scheme and Syllabus, Credits was fixed to 200
 - PG 2018-2020 Scheme and Syllabus, Credits was fixed to 88
4. Salient Aspects Discussed for UG 2018-22 Scheme and Syllabus:
 - 2018-22 Scheme was presented by HoD.

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- Dr. Ravish Aradhya from RVCE suggested that System Verilog and Algorithms for CAD Tools can be offered as elective.
- Dr. S. L. Pinjare suggested System Verilog needs to include verification aspects. He suggested referring books by Saran and Ima for System Verilog.
- Dr. Praveen B from Samsung was happy with the introduction of ARM Microcontroller in 4th semester. He was in the opinion that it is much required to meet present industry requirements and placements.
- 2018-22 Scheme and Syllabus from 3rd to 4th semester was approved by all the panel members of the committee. The syllabus was deemed satisfactory.
- There is no revision made in 1st year Basic Electronics syllabus for 2018-22 Scheme.

5. Salient Aspects Discussed for UG 2017-21 Scheme and Syllabus

- 2017-21 Scheme was presented by HoD. Newly introduced subjects and subjects with major changes were presented.
- **Subjects with major/minor changes were as discussed:**
 - Subjects, on Data Structures using C++ in 5th semester and Computer Communication Network in 6th semester includes hands on experiments starting from the academic year 2019-20. This was agreed upon by the panel and very much appreciated by Dr. Ravish Aradhya.
 - In Control Systems PD, PI and PID controller concept is added as per suggestion from previous 2018-19 BoS meeting held on 16/6/2018.
 - Radar concepts are introduced in Microwave Engineering and the subject is renamed to Microwave Engineering and RADAR.
 - Design based experiments were included in DSP Lab by Dr. H S Prashanth and this was agreed by the panel.
 - Alumni member Mourya Prashanth was of the opinion documentation was very important in industry and training must be given to students regarding good documentation of lab experiments. Further students must also be taught to create libraries and reuse them.

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- Alumni member Sandeep K suggested tool based assignment must be made mandatory at least for one subject per semester. Plagiarism check should be carried out even for **mini project** and students must be encouraged to use open source tool for assignments and mini projects. He also suggested students must be involved in interdisciplinary projects. However this was clarified by HoD, that most of the projects carried out in the Centers of Excellence were of interdisciplinary nature.
- Praveen B highly appreciated the process in which BoS was conducted. He said conducting prior internal BoS multiple times, collecting justification for changes made, consolidating the changes and presenting before the panel was a tedious task and this has been carried out well. He suggested including industry based lab for subjects like **Automotive Electronics, RTOS etc.**
- Praveen B also suggested that AGILE based evaluation must be done for major projects. But this was not accepted by the panel.
- Dr. Ravish Aradhya suggested including scripting in **VLSI Lab.**
- The panel agreed upon adding network security topics to Cryptography.
- **New Electives/Subjects were as discussed:**
 - HOD presented the new subjects/ electives offered across semesters. The new subjects were introduced based on focused research areas of department, current industry and technology trends and placement needs.
 - **Semiconductor Devices and Nano Electronics** is introduced as a program elective in 5th semester. The subject syllabus was presented by Dr. Rajan K Pandey. Dr. Ravish Aradhya suggested removing overlap in **Unit 4 and 5 on MOSFET**, as this was previously covered in Analog Electronic Circuits.
 - **Biomedical Signal Processing** is introduced as a program elective in 7th semester. The subject syllabus was presented by Ms. Manjula B M., Dr. Ravish Aradhya and Mr. Praveen B suggested including 50Hz adaptive filter design in Unit 3. Concept on EEG must be covered in previous unit

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before offering it as case study in Unit 5. Machine Learning for Pattern Recognition must be made a prerequisite for this subject.

- **Applied DSP** is introduced as a program elective in 7th semester. The subject syllabus was presented by Dr. Rajesh N. The syllabus was agreed by the panel members.
- **Systems Engineering in Space Crafts** is introduced as an open elective in 7th semester. The subject syllabus was presented by Prof. G V C Rajan. The panel suggested changing the 3rdCO. Praveen B suggested including power management optimization techniques in Unit 3 and including power subsystems in Unit 2.
- **Software Defined Radio** is introduced as a program elective in 6th semester. The subject syllabus was presented by Dr. S Sandya. Dr. Ravish Aradhya suggested including Hands on Experiments.
- Apart from the suggested minor changes 2017-21 Scheme and Syllabus from 5th to 8th semester was approved by all the panel members of the committee. The syllabus was said to be satisfactory.
- The panel suggested to provide the list of **MOOC based electives** at the time at which the electives were to be offered.

6. Salient Aspects Discussed for UG 2014-17 Scheme and Syllabus

- 2014-17 Scheme was presented by HoD. Newly introduced electives were presented.
 - **Applied DSP** is introduced as a program elective in 7th semester.
 - **Biomedical Signal Processing** is introduced as a program elective in 7th semester.
 - **Software Defined Radio** is introduced as a program elective in 7th semester.
 - **Machine Learning for Pattern Recognition** is introduced in 6th semester. The syllabus was agreed by the panel members. However it was suggested by the panel to include Python based hands on assignments.

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- 2014-17 Syllabus from 7th to 8th semester was approved by all the panel members of the committee.

7. Salient Aspects Discussed for PG 2018-20 Scheme and Syllabus

- 2018-20 Scheme and Syllabus of VLSI Design and Embedded System and DCN were presented by HoD.
 - Praveen B suggested in not offering Mathematics for PG. But Dr. Padmavathi N defended it, saying that was the pre requisite for subjects like Machine Learning, Digital Communication and DSP.
 - Praveen B suggested that internship for PG students must be monitored more rigorously. PG students must contribute more towards in-house interdisciplinary projects.
 - Dr. Ravish Aradhya suggested to make hardware based design a must for major projects.
 - 2018-20 Scheme and Syllabus of both the programs were accepted by the panel members.

SEE Co-ordinator

Yashu Prasad



HoD, ECE
Head,

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ADVANCED MICROCONTROLLER

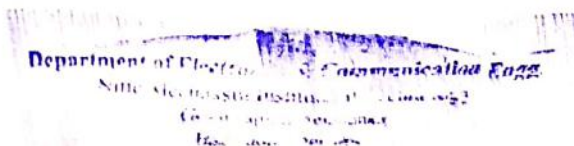
Course Code	17EC45	Credits	04
Hours/Week(L-T-P)	4-0-2	CIE Marks	50
Total Hours	39(L)	SEE Marks	50
Exam Hours	03	Course Type	Core

COURSE OUTCOMES	
1.	Students will get exposure to the higher architecture of an advanced microcontroller
2.	Students will get introduced to the diverse instructions that an advanced microcontroller supports
3.	Students will understand the role of tools and libraries in the software implementation for an advanced microcontroller
4.	Students will go through the steps involved in programming the peripherals present in an advanced microcontroller

COURSE CONTENTS	
UNIT-1 (8Hrs)	
ARM Cortex M3: ARM Cortex M3 Processor and ARM Family, Cortex-M3 Processor Applications, Architecture of ARM Cortex M3, Operation Modes, The built-in nested Vectored Interrupt Controller, Memory Map, The Bus Interface, The MPU, Low Power and High Energy Efficiency, Debugging Support Text: 1.1, 1.2, 1.5, 2.1, 2.3, 2.4, 2.5, 2.6, 2.7, 2.9.1, 2.10 ARM Cortex M3 Architecture: Registers, Special Registers, Vector Tables, Stack Memory Operation, Reset Sequence Text: 3.1, 3.2, 3.5, 3.6, 3.7	
UNIT-2 (8Hrs)	
ARM Cortex M3 Instruction Set: Assembly Basics, Instruction List, Instruction Descriptions, Several Useful Instructions in the Cortex M3 Text: 4.1, 4.2, 4.3, 4.4, 4.5, 4.6 ARM Cortex M3 Memory Systems: Memory System Features Overview, Memory Map, Memory Access Attributes, Memory Access Permissions, Bit-Band Operations, Unaligned Transfers, Exclusive Access, Endian Mode Text: 5.1, 5.2, 5.3, 5.4, 5.5, 5.6	
UNIT-3 (8Hrs)	
ARM Cortex M3 Exceptions: Exception Types, Definition of Priorities, Vector Tables, Interrupt Inputs and Pending Behaviour, Fault Exceptions, Supervisor Call and Pendable Service Call Text: 7.1, 7.2, 7.3, 7.4, 7.5, 7.6 ARM Cortex M3 NVIC: Nested Vectored Interrupt Controller Overview, The Basic Interrupt Configuration, Example Procedures in Setting Up an Interrupt, Software Interrupts, The SYSTICK Timer Text: 8.1, 8.2, 8.3, 8.4, 8.5, 8.6	
UNIT-4 (8Hrs)	
ARM Cortex M3 Programming: Overview, A Typical Development Flow, Using C, CMSIS, Using Assembly, Using Exclusive Access for Semaphores, Using Bit Band for Semaphores, Working with Bit Field Extract and Table Branch Text: 10.1, 10.2, 10.3, 10.4, 10.5, 10.6	

Approved
V. J. S.
 14-3-19

A. Sanyal
 11/3/19



S. Sridhar
 11/3/19

UNIT-5 (7Hrs)

ARM Cortex M3 MPU and Other Features: MPU Registers, Power Management, Multiprocessor Communication, Self-Reset Control

Text: 13.2, 14.2, 14.3, 14.4

ARM Cortex M3 Debug Architecture: Debugging Features Overview, Core Sight Overview, Debug Modes, Debugging Events, Text: 15.1, 15.2, 15.3, 15.4

TEXT BOOKS

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3, Newnes, (Elsevier), 2008

REFERENCE BOOKS

1. David Patterson and John L. Hennessey, "Computer Organization and Design". (ARM Edition), Morgan Kauffman.

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSEMENT METHOD

CIE:

1. Two Surprise Tests. 10 Marks each. Best of two tests will be taken.
2. Assignment course project based test. 10 Marks each. Best of two tests will be taken.
3. Three internals. 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	*	*	*					*		*					
CO2		*	*	*		*				*	*				
CO3	*			*			*			*					
CO4		*	*					*		*					

Approved
Vijal
Permitted to take approval from next BOS.
Vijal
14.3.19

Samy J
11/3/19

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SEMESTER: VI

MACHINE LEARNING FOR PATTERN RECOGNITION

Course Code	14ECE659	Credits	04
Hours/Week(L-T-P-S)	4-0-0-0	CIE Marks	50
Total Hours	45	SEE Marks	50
Exam Hours	03	Course Type	Core Elective

COURSE OUTCOMES	
Co	CO Statements
1	Explain the machine learning framework and establish the wide ranging application of machine learning
2	Demonstrate the working of Machine learning techniques.
3	Illustrate a few algorithms in machine learning.
4	Apply appropriate machine learning techniques for real time applications as per the scope of the applications learned.
5	Develop skills of using recent machine learning software for solving real time practical problems

COURSE CONTENTS	
UNIT-1 (9 Hrs)	
INTRODUCTION TO MACHINE LEARNING Introduction, Machine perception, Pattern Recognition systems: Sensing, Segmentation and Grouping, Feature Extraction, Classification, Post Processing. The Design cycle: Data Collection, Feature choice, Model choice, Training, Evaluation and Computational Complexity. Learning and Adaptation: Supervised Learning, Unsupervised Learning, Reinforcement Learning. Learning Problems, Designing Learning systems, Perspectives and Issues in Machine Learning. An overview of matrices operations in image processing (Text-1-CH1: 1.1 to 1.5, Text-1-CH1:1.1 to 1.3)	
UNIT-2 (9 Hrs)	
LINEAR MODELS FOR REGRESSION Curve Fitting, Linear Basis Function models: Maximum Likely hood and least squares, Geometry of least squares, Sequential learning, Regularized least squares, Multiple outputs. Bias-Variance Decomposition, Bayesian Linear Regression: Parameter distribution, Predictive distribution, Equivalent kerne.(Text-3-CH 3: 3.1 to 3.3)	
UNIT-3 (9 Hrs)	
CONCEPT LEARNING AND DECISION TREES Concept Learning, Version Spaces and Candidate Elimination Algorithm, Inductive Bias, Decision Tree learning: Representation, Algorithm, and Heuristic Space Search. (Text-2-CH-2: 2.1, 2.2, 2.5 and 2.7 & CH- 3:3.1, 3.2, 3.4 and 3.5)	
UNIT-4 (9 Hrs)	
ARTIFICIAL NEURAL NETWORKS Neural Network Representation, Problems, Perceptrons, Multilayer Networks and Back Propagation Algorithms, Genetic Algorithms, Hypothesis Space Search, Genetic Programming. Models of Evolution and- Genetic Algorithms; Hypothesis Space Search, Genetic Programming; Models of Evolution and Learning. (Text-2-CH-4: 4.2, 4.3, 4.5 and 2.7 & CH- 9: 9.2, 9.4, 9.5 and 9.6)	
UNIT-5 (9 Hrs)	
IMAGE AND SPEECH BASED MACHINE LEARNING Review of algorithms related to image processing, speech recognition, application of digital image	



processing approaches in machine learning environment (Ex. Latest approaches like enterprise image processing, pattern recognition approaches used in AI etc. will be used). (Case Study, No book).

TEXT BOOKS

1. Richard O. Duda, Peter E. Hart and David G. Stork "Pattern Recognition and Machine Learning", Christopher M. Bishop, 2006 Springer Science+ Business Media, LLC John Wiley, 2001.
2. Tom M. Mitchell, "Machine Learning", McGraw-Hill Education (INDIAN EDITION), 2013
3. Christopher M. Bishop, "Pattern Recognition and Machine Learning", 2006 Springer Science+ Business Media, LLC

REFERENCE BOOKS

1. Ethen Alpaydin, "Introduction to Machine Learning", 2nd Ed., PHI Learning Pvt. Ltd., 2013
2. Eart Gose, Richard Johnsonburg and Steve Joust, "Pattern Recognition and Image Analysis," Prentice-Hall of India, 2003.
3. Damodar N. Gujarati, "Basic Econometrics" MC GRAWHILL, USA
Software for coding/modelling: R, Python and Matlab.

TEACHING METHODOLOGY

- Lectures, Problem Based Learning
- Discussion
- Demonstration
- Illustration

COURSE ASSESMENT METHOD

CIE:

1. Tutorials - 10 Marks
2. Surprise tests - 10Marks.
3. Three mid examinations, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit
- Final examination of 100 Marks will be conducted and will be evaluated for 50 Marks

CO-PO-PSO MAPPING

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	S	S	M	S	S	S	S	W	M	S	S	M	W	W	S
CO2	S	S	W	S	S	S	S	W	S	S	S	M	W	W	S
CO3	S	S	S	S	S	M	M	M	S	M	M	S	W	W	S
CO4	S	S	S	S	S	M	S	M	S	M	S	S	W	W	S
CO5	S	S	S	S	S	M	M	W	S	M	S	S	W	W	S

Approved
V. Sidu
14/3/19

P.T.K

Sanku
2/1/19

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Sensors and Actuators

Sub: Sensors and Actuators

Credits: 3
L.T.P: 3.0.0

Sub Code: 14ECO661

Semester:6

Unit	Old	New
1	<p>Unit 1: Introduction: Motivation ,Definition Of Sensor And Actuator, Domain Of Physical Phenomena, Classification Of Sensors And Actuators ,</p> <p>Micro And Nano-Technologies : Introduction , Manufacture</p> <p><i>Text Book 1: Chapter 1&2</i></p>	<p><i>It is retained</i></p>
	<p>Based On The Electric Field: Force, Electric Field And Voltage, Concept Of Capacity ,Capacitive Displacement Sensor, Capacitive Acceleration Sensor , Electrostatic Loudspeaker ,Electrostatic Mems Actuator, Definition Of Electric Resistor, Potentiometric Displacement Sensors, Dependence Of Resistivity With Temperature And Moisture, Resistive Temperature Detector, Thermistor Integrated Temperature Sensor, Dependence Of Resistivity With Deformation ,Strain Gage</p> <p><i>Text Book 1: Chapter 3</i></p> <p><i>Text book used: SMART SENSORS AND ACTUATORS, Francisco Andre Correa Alegria, 2014</i></p>	<p>Instrumentation of an Engineering System: Role of Sensors and Actuators, Application Scenarios, Human Sensory System, Mechatronic Engineering, Control System Architectures, Instrumentation Process</p> <p>Component Interconnection and Signal Conditioning: Introduction; Component Interconnection Signal Modification and Conditioning.</p> <p><i>Reason: The text book followed earlier was not a standard text book. It was master thesis of a student. It had errors in notations like corrosion being used in place on etching. The English language used was also not appropriate. Hence from second unit on wards the following text book has been referred</i></p> <p>Text book: Sensors and Actuators Engineering System Instrumentation, Clarence W. de Silva, 2nd Edition, CRC Press</p>

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<p>Unit III</p> <p>Based On Mechanical Phenomena: Piezoelectric Effect, Accelerometer, Piezoelectric Temperature Sensor , Acoustic Waves, Ultrasound Transducers, Measuring Distance Using Ultrasound (Sonography, Sonar, Etc...), Fluid Actuators</p> <p><i>Text book used:</i> SMART SENSORS AND ACTUATORS, Francisco Andre Correa Alegria, 2014</p>	<p>Analog Sensors and transducers: Sensors and Transducers, Sensors for Electromechanical Applications, Potentiometer, Variable-Inductance Transducers, Permanent-Magnet and Eddy Current Transducers, Variable-Capacitance Transducers, Piezoelectric Sensors, Strain Gauges, Torque Sensors, Gyroscopic Sensors, Thermo-Fluid Sensors</p> <p>Text book: Sensors and Actuators Engineering System Instrumentation, Clarence W. de Silva, 2nd Edition, CRC Press</p>
<p>Unit IV</p> <p>Based On Thermal Phenomena: Thomson Effect, Peltier Effect, Seebeck Effect, Thermocouple, Peltier Cell, Joule Effect, Guckel Thermal Actuator , Hot Wire Anemometer</p> <p><i>Text book used:</i> SMART SENSORS AND ACTUATORS, Francisco Andre Correa Alegria, 2014</p>	<p>Digital and Innovative Sensing: Innovative Sensor Technologies, Shaft Encoders, Incremental Optical Encoder, Motion Sensing by Encoder, Miscellaneous Digital Transducers, Optical Sensors, Lasers, and Cameras, Miscellaneous Sensor Technologies (except problems on the same), Tactile Sensing, MEMS Sensors, Wireless Sensor Networks</p> <p>Text book: Sensors and Actuators Engineering System Instrumentation, Clarence W. de Silva, 2nd Edition, CRC Press</p>
<p>Unit V</p> <p>Based On Electromagnetic Radiation: Quantities And Units, Electroluminescence, Photovoltaic Effect, Led, Photoresistor , Photodiode, Pyrometers, Source Of X-Rays, Measurement Of The Blood Oxygen Level With A Pulse Meter, Computer Optical Mouse, Wii Game Console, X-Ray Computed Tomography, Multi-Touch Screen, Global Positioning System (Gps)</p> <p><i>Text book used:</i> Nathan Ida Sensors, Actuators, and their Interfaces: A Multidisciplinary Introduction SciTech Publishing 2013</p>	<p>Continuous - Drive Actuators: Introduction, DC Motors, Control of DC Motors, Motor Driver and Feedback Control, DC Motor Selection, Induction Motors, Synchronous Motors, Linear Actuators, Hydraulic Actuators, Pneumatic Control Systems, Fluidics</p> <p>Text book: Sensors and Actuators Engineering System Instrumentation, Clarence W. de Silva, 2nd Edition, CRC Press</p>

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DEPT OF ECE

PROPOSED BOARD OF STUDIES PANEL 2018-19

14/7/2018

The nominated UG & PG BOS panel members for the year 2018-19 are as follows:

Sl No.	Name	Designation	Affiliation
1.	Dr.Sandya S	Chairperson	Professor & Head, Dept. of ECE, NMIT, Bengaluru
2.	Dr N C Shivaprakash	Member (VTU Nominee)	Chief Research Scientist, IISc, Bangalore
3.	Dr Ravish Aradhaya	Member (Academic Expert)	Professor, Dept. of ECE, RVCE, Bangalore
4.	Mr. Somashekhar Basavaraj	Member (Industry Expert)	Co-founder of CEO, Analog semi.
5.	Mr. Chanakya K V	Member (Alumni)	Lead EDA Engineer Texas Instruments India.
6.	Faculty Members ECE	Member	NMIT, Bangalore
7.	Ms Varsha Prasad	Member Secretary	Assoc. Prof, Dept. of ECE, NMIT


Dr S Sandya

HOD, ECE

Head,

Department of Electronics & Communication Eng

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Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 30/04/2018

Following are the Panel members for Subject : **Advanced Microcontroller Lab, IV SEM**

REVIEWER: Prof. Sankar Dasiga

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Mr. Sankar Dasiga	Prof. Sankar Dasiga	Power Electronics lab 10.00 A.M
2	Mr. Girish G K		
3	Ms. Ayesha		

Following points were discussed

1. As per the industry need, Advanced microcontroller lab (ARM CORTEX M4) was introduced
2. Prof. Sankar Dasiga (Expert faculty) and subject teachers prepared a draft document of list of experiments
3. The draft copy of lab syllabus was discussed and approved.

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HoD, ECE
(Signature)
30/4/18
(Dr. Sandhya S)
Head,
Department of Electronics & Communication Engg
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Nitte Meenakshi Institute of technology

Yelahanka, Bangalore

Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 30/04/2018

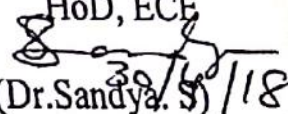
Following are the Panel members for Subject : **Advanced Microcontroller, IV SEM**

REVIEWER: Prof. Sankar Dasiga

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Mr. Sankar Dasiga	Prof. Sankar Dasiga	Power Electronics lab 10.00 A.M
2	Mr. Girish G K		
3	Ms. Ayesha		

Following points were discussed

1. As per the industry need, **Advanced microcontroller subject (ARM CORTEX M3) was introduced.**
2. Prof. Sankar Dasiga (Expert faculty) and subject teachers prepared a draft document with Prerequisites, Syllabus, COs, Evaluation Methodology etc
3. The draft syllabus was discussed and approved.

HoD, ECE

(Dr. Sandya. S) / 18

Head,
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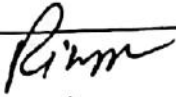
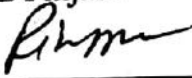

Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 3/12/2018

Following are the Panel members for Subject : **Sensors and Actuators**

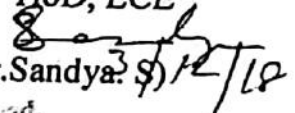
REVIEWER: Dr S L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Dr S L Pinjare 	Dr S L Pinjare 	R & D lab
2	Dr Veda 		10.30 A.M

Following points were discussed

The textbook followed earlier was not a standard textbook. It was a master thesis of a student. It had errors in notations like corrosion being used in place on etching. The English language used was also not appropriate. Hence from second unit onwards Sensors and Actuators Engineering Systems Instrumentation, Clarence W.de.Silva, 2nd Edition, CRC Press text book has been referred .

HoD, ECE


(Dr. Sandya S) 3/12/18

Head,

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Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 30/04/2018

Following are the Panel members for Subject : ~~Linear Integrated Circuits, IV SEM~~

REVIEWER: Dr.S.L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Ms.Bhuvaneshwari	Ms. Bhuvaneshwari	Project lab 10.00 A.M
2	Ms.Savithri		
3	Dr.Veda		

Following points were discussed

1. No changes are required in unit 1.
2. In unit 2 high impedance circuits are removed as its significance is not much.
3. In unit 3 signal processing circuits are to be learnt before application of op amp. Also same book is continued as this gives good flow in the subject.
4. In unit 4 Signal generators are now introduced after understanding differentiator and integrator circuits. And V I converters are already covered in second unit, hence removed from this unit.
5. No changes are required in unit 5.


30/HOD, ECE

(Dr.Sandya. S)

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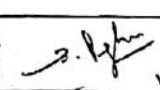
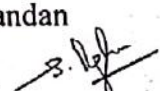

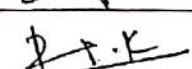
Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 3/12/2018

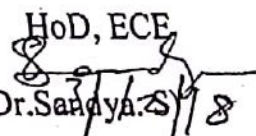
Following are the Panel members for Subject: Machine Learning for Pattern Recognition

REVIEWER: Dr Raghunandan

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Dr.Raghunandhan 	Dr Raghunandan 	R & D lab
2	Dr.Jayavrinda 		10.30 A.M
3	Mr.Ravindra 		

Following points were discussed

1. As per the industry need, Machine Learning for Pattern Recognition subject is proposed to offer as Core Elective for 6th sem for the year 2018-2019.
2. The draft copy of lab syllabus was discussed and approved.

HoD, ECE

(Dr. Sandya S)

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



Department of Electronics and Communication Engineering

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Date: 30/04/2018

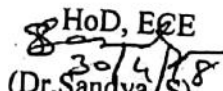
Following are the Panel members for Subject : **Network Analysis, III SEM**

REVIEWER: Dr.S.L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Ms. Deeksha R shetty 	Ms. Manjula B M 	Project lab
2	Ms. Manjula B M 		10.00 A.M
3	Mr. Girisha G K 		

Following points were discussed

1. No changes are required in unit 1.
2. Suggested to swap unit 3 with unit 2.
3. **Basics of Laplace student** will study in maths. Hence a new topic is included in unit 4.
4. Suggested to swap unit 4 with unit 2.
5. No changes are required in unit 5.


HoD, ECE
(Dr. Sandya S)

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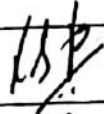



Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 30/04/2018

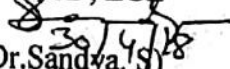
Following are the Panel members for Subject : **Digital design using Verilog, IV SEM**

REVIEWER: Dr.S.L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Ms. Rekha 	Dr.S.L Pinjare 	Project lab
2	Mr. Shashidara 		10.00 A.M
3	Ms. Deeksha R Shetty 		

Following points were discussed

1. In unit 1, text book changed from Bhaskar to Stephen Brown.
2. **In unit 2, topics from unit 1 of old syllabus is shifted to Unit 1 in new syllabus** along with extra topics from Samir Palnitkar.
3. In unit 3 and unit 4 topics reframed.
4. In unit 5, text book changed and topics reframed and new topics added.

HoD, ECE

(Dr. Sandya S)
Head,

Department of Electronics & Communication Engg
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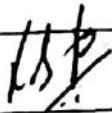



Department of Electronics and Communication Engineering

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Date: 30/04/2018

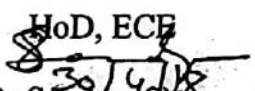
Following are the Panel members for Subject : ~~Digital design using Verilog, IV SEM~~

REVIEWER: Dr.S.L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Ms. Rekha 	Dr.S.L Pinjare 	Project lab
2	Mr. Shashidara 		10.00 A.M
3	Ms. Deeksha R Shetty 		

Following points were discussed

1. In unit 1, text book changed from Bhaskar to Stephen Brown.
2. ~~In unit 2, topics from unit 1 of old syllabus is shifted to Unit 1 in new syllabus,~~ along with extra topics from Samir Palnitkar.
3. In unit 3 and unit 4 topics reframed.
4. In unit 5, text book changed and topics reframed and new topics added.


(Dr. Sandya S)
Head,

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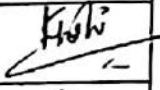

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Internal BOS Meeting

Date: 30/04/2018

Following are the Panel members for Subject : **Digital Electronics, III SEM**

REVIEWER: Dr.S.L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Ms.Binu Singh	Ms. Binu Singh	Project lab
2	Ms. Kushalatha M R 		10.00 A.M
3	Ms. Deeksha R Shetty 		

Following points were discussed

1. The basics of combinational logic will be covered in the First Unit
2. To meet the requirements of the **DE lab**, all the **combinational topics are planned to be covered in the first two units**
3. Thus include the sequential circuits in units 3 , 4 and 5


30/4/18
HoD, ECE

(Dr.Sandya. S)

Head,

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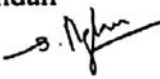
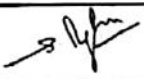
Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 30/04/2018

Following are the Panel members for Subject : **Digital Signal Processing, IV SEM**

REVIEWER: Dr.Raghunandan

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Mr.Shashidhar K S 	Dr.Raghunandan 	DCN lab
2	Dr.Raghunandan 		10.00 A.M
3	Mr. Rajesh.N		

Following points were discussed

1. Text book that will be appropriate for DSP course (UG), and concluded that the book "Digital Signal Processing" by Oppenheim and Schafer is suitable for this purpose.
2. The reason for this change is that while the book by Oppenheim and Schafer is equally good and well-known, it can provide continuity to the students in terms of notations, style of presentation, etc. because of the preceding course on Signals and Systems (which uses the book by the same authors).


30/4/18
HoD, BCE

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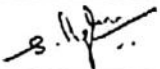

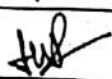
Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 3/12/2018

Following are the Panel members for Subject : **Digital Image Processing**


REVIEWER: Dr Prashanth H S

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Dr.Raghunandhan 	Dr Prashanth H S 	R & D lab
2	Dr Prashanth H S 		10.30 A.M

Following points were discussed

As per the industry need **Digital Image Processing** subject is proposed to offer as Core Elective for 6th sem for the year 2018-2019.

1. The draft copy of lab syllabus was discussed and approved.

HOD, ECE

(Dr. Sandya)

Head,
Department of Electronics & Communication Engg
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Internal BOS Meeting

Date: 30/04/2018

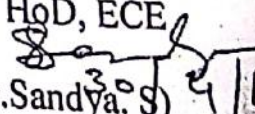
Following are the Panel members for Subject : **Analog Electronics Circuits, III SEM**

REVIEWER: Dr.S.L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1.	Ms. Beena S Rai 	Ms. Smitha	Project lab 10.00 A.M
2.	Ms. Sowmya J 		
3.	Ms. Bhuvaneshwari 		

Following points were discussed

1. Few topics from second unit are included in unit 1 for continuation.
2. **In Unit 2 and 3 concepts based on BJTs are obsolete, the same are replaced by JFET and MOSFET respectively.**
3. In addition to Feedback circuits, Oscillators concepts are added are introduced in unit 4.
4. In addition to Power Amplifiers, concepts of Voltage regulators are added are introduced in unit 5.

HoD, ECE

(Dr. Sandya S) 30/4/18

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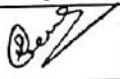

Department of Electronics and Communication Engineering

Internal BOS Meeting

Date: 30/04/2018

Following are the Panel members for Subject : **AEC LAB, III SEM**

REVIEWER: Dr.S.L Pinjare

SL NO	Subject Teachers	Expert Faculty	Venue & Time
1	Mr. Girish G K 	Ms. Bhuvaneshwari	Project lab 10.00 A.M
2	Ms. Beena S Rai 		
3	Ms.Sowmya.J 		

Following points were discussed

1. Experiment No. 5, 6, 7 are FET based experiments. Since, Transistors are obsolete, the above experiments are introduced.
2. Experiment No. 9 is changed from Transistor based oscillator to FET Based oscillator.
3. Experiment No. 7, 9 & 10 are removed from 2014-17 syllabus and Experiment No. 3 & 8 are added in 2017-21 syllabus.

HoD, ECE


(Dr. Sandya. S)

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NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ECE

BOARD OF STUDIES

PANEL MEMBERS

ACADEMIC YEAR: 2018-2019 (JUNE)

Date of BoS meeting	16 th JUNE 2018
BOS External Members	<ol style="list-style-type: none">1. Dr.Rathna C.N Principal Research Scientist, IISc, Bangalore2. Dr.Abhay Deshpande, Assoc.Prof, RVCE, Bangalore3. A Jegan, Senior Engineer, KPIT, Bangalore
BOS Internal Memebers	<ol style="list-style-type: none">1. Dr.Sandya S2. Prof.Mahaveer Swamy3. Dr.S.L.Pinjare4. Dr.Raghunandhan5. Prof .Sankar Dasiga6. Prof.Sitram Yaji7. Dr.Veda8. Ms.Manjula
Alumini	<ol style="list-style-type: none">1. Savithri Hande2. Mourya Prashanth
DUGC Coordinator	<ol style="list-style-type: none">1. Ms.Deebalakshmi
BOS Coordinators	<ol style="list-style-type: none">1. Varsha Prasad2. Pramodhini R3. Sowmya J

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Bangalore - 560 064



TITLE: Minutes of Meeting	DESCRIPTION: External BOS	Year: 2018	Date: 16/6/18	Page 1/1
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External BOS (UG and PG) meeting was held on 16/6/2018 from 9.00AM to 12PM in R&D Lab.

AGENDA:

The agenda for the BOS meeting is:

- UG scheme for 2017-2021 batch.
- 1st year scheme for 2018- 2022 batch.
- Review of subject contents of 2nd year (3rd and 4th Sem) for 2017-2021.
- PG scheme for 2018 – 2020.

External Panel Members

SI No	Name of the Member	Designation	Domain Expertise
1	Dr Shankarananda	VTU Nominee	
2	Dr Rathna C N	Principal Research Scientist, IISc, Bangalore	Signal and Image Processing
3	Dr Abhay Deshpande	Assoc.Prof, Department of ECE, RVCE, Bangalore	VLSI
4	Mr. Jegan	Senior Engineer, KPIT, Bangalore	Embedded Systems

Internal Panel Members

SI No	Name of the Member	Designation	Domain Expertise
1	Dr. S. Sandya	Professor and Head, Chairperson, BoS	Embedded Systems and Satellite Communication
2	Prof.Mahaveer Swamy	Professor	Fiber optics, Wireless and Satellite Communication
3	Dr.S.L.Pinjare	Professor	VLSI and MEMS
4	Dr. Raghunandhan	Professor	Internet of Things, Multimedia, Machine learning
5	Prof. SankarDasiga	Professor	Computer Communication and Networking , Embedded Systems
6	Prof. SitaramYaji	Professor	Embedded system software and IP (IPv4/IPv6) Networking

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	Dr Veda	Associate Professor	MEMS Device Solutions
8	MsManjula	Associate Professor	Fault Tolerant System Design
9	Dr Revathi	Associate Professor	Mathematics

Alumni Panel members

- MouryaPrashanth (UG)
- SavithriHande (PG)

Minutes of Meeting (UG and PG)

1. HOD briefed on the Agenda of BOS meeting.
2. There was a revision in Scheme and Syllabus of :
 - UG 2017-2021 Scheme and Syllabus, Credits was fixed to 200
 - UG 2018-2021 Scheme and Syllabus (only first year), Credits was fixed to 175
 - PG 2018-2020 Scheme and Syllabus, Credits was fixed to 72
3. HOD explained the steps taken to frame the scheme and syllabus by the internal faculty. The steps are:
 - January 2018 started the process of identification of the subjects required
 - February Internal BOS was conducted and teams were formed with experts to review on syllabus of the subjects
 - April & May 2018 finalizing of the contents to present to BOS

Minutes of Meeting for UG (2017-2021; 2018-2022 Scheme)

SI No		Action Items
1.	Dr. Abay Deshpande from RVCE suggested that third semester Microprocessor should be taught to understand DSP better. But Prof. Sankar clarified syllabus in microcontroller contains a unit covering CISC and RISC architecture and introduction is provided to microprocessor architecture.	Prof Sankar and Mr. Girish (Unit 1 of Microcontroller should include introduction to microprocessor architecture)
2.	Mr. Jegan from KPIT raised his concern of having Network analysis and AEC in the same semester as Networks Analysis form the prerequisite for AEC. Also the same concern for Digital Electronics and Microcontroller. HOD gave justification that Basic Electronics covers pre-requisites	

	required for of Digital Electronics, Analog Electronic Circuits and Network Analysis.	
3.	<p>Dr. Rathna from IISC, felt students may find it difficult having DSP, Advanced Microcontroller and Fields & Waves in the same semester.</p> <p>Our Alumni Maurya was happy with this change, as students get idea of different flavors which helps them to choose their final project.</p>	
4.	Mr. Jegan suggested that Microcontroller, subject must include certain hands on session on 8051. He suggested Demos or Lab / Hands-on exercises using TinkerCAD / circuits.io / Proteus / EdSim51 for Microcontroller.	Mr Girish
5.	<p>Dr Abhay Deshpandade, was of the opinion that Data Structures must be an Elective subject in Electronics.</p> <p>Prof. Sankar and Prof. Yaji justified that it is much required to fulfill industry needs.</p>	
6.	Mr Jegan said syllabus must explicitly indicate if optimization techniques are used.	All faculty members
7.	Mr Jegan suggested that "Automotive Electronics" must be offered as elective during the 5th or 6th semester.	All faculty members
8.	<p>It was suggested that we introduce / include the following technologies / topics in our UG courses:</p> <ol style="list-style-type: none"> i. Communication Protocols: SPI, I2C, UART, Ethernet, CAN (Advanced Microcontroller) ii. Embedded C (Advanced Microcontroller) iii. Last-mile Wireless Communication Technologies – BT, Zigbee, NFC (CCN) iv. Cyber Security (Cryptography) v. Kalman Filter – SW implementation of (DSP) vi. PWM, PID / PI / PD Controllers – SW implementation of (Control Systems) vii. OpenSSL (Cryptography or CCN) viii. OS Fundamentals (There should be a core 	All faculty members

	<ul style="list-style-type: none"> ix. Aspects of development of Android Applications x. AUTOSAR (Automotive Electronics) xi. Programming with C++, Python 	
9.	<p>Discussion on Electives:</p> <ul style="list-style-type: none"> a. HOD explained the flow of electives where a student can grow on his area of interest. b. Image processing is covered in Multimedia 1 and Multimedia 2. c. Suggested by BOS to introduce scripting tool for VLSI d. ANN can be renamed as Fuzzy Logic and soft computing. e. To consider System Engineering to be introduced elective. f. Identify VLSI based MOOC courses. 	All faculty members
10.	Dr Rathna suggested that Cryptography syllabus to be modified to include cyber security. Also to rename the subject.	Ms Rekha

Minutes of Meeting for PG (2018-2020 Scheme for VLSI and DCN)

SI No.		Action Items
1.	HOD introduced the course flow and credits.	
2.	Mr. Jegan from KPIT suggested that "Automotive Electronics" can be offered as an elective course in our M Tech DCN as well as ES & VLSI courses.	Prof Sankar
3.	Dr Rathna suggested there should be an elective course on <u>Machine Learning</u> in UG and PG.	Prof Raghunandan
4.	Dr Rathna suggested there should a course on Wireless Mobile Networks offered for PG DCN.	Prof Raghunandan
5.	Students should be exposed to hands on with RPi 3 and a board with an ARM Cortex MCU	PG Faculty Members

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Extensive hands-on exposure to Matlab is suggested to both the UG and PG students.

BoS Co-ordinators:

Vasle P
Prasad M
Sowmya J

DUGC Co-ordinators:

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21/6/18
Dr. S. Sandya

HoD, Dept. of ECE

Head,
Department of Electronics & Communication Engg
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 084

NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPT OF ECE

Panel Members of UG BOARD OF EXAMINERS MEETING March-2018

Date: 19/3/2018

External BoE

Sl no	Name	Designation	College	Signature
1	Dr.Rangaraju H.G.	Professor	GSKSJTJ	<i>[Signature]</i> 19/3/18

Internal BoE

Sl no	Name	Designation	Signature
1	Dr.Sandya S	Professor	<i>[Signature]</i> 19/3/18
2	Dr.Raghunandha	Professor	<i>[Signature]</i> 19/3/2018
3	Dr.S.L.Pinjare	Professor	<i>[Signature]</i> 19/3/2018
4	Prof MahaviraSwamy	Professor	<i>[Signature]</i> 19/3/2018
5	Dr.Lalitha Y S	Professor	
6	Prof.Sankar Dasiga	Professor	<i>[Signature]</i> 19/3/18
7	Prof.Sitaram Yaji	Professor	<i>[Signature]</i>
8	Dr.Veda	Assoc. Prof	<i>[Signature]</i> 19/3/2018
9	Mr.Rajesh . N	Assoc. Prof	<i>[Signature]</i>
10	Ms.Manjula	Assoc. Prof	<i>[Signature]</i> 19/3/18
11	Ms.Madhu patil	Assoc. Prof	<i>[Signature]</i> 19/3/18
12	Mr.Prasanna paga	Assoc.Prof	<i>[Signature]</i> 19/3/18
13	Mr.Shashidhar K S	Assoc.Prof	<i>[Signature]</i> 19/3/18
14	Ms.Rekha	Asst.Prof	<i>[Signature]</i> 19/3/18

HoD,ECE

[Signature]
(Dr.Sandya S)/19/3/18

Head,
Department of Electronics & Communication Engg
Nitte Meenakshi Institute of Technology
Gowdapura, Yelahanka
Bangalore - 560 062

Subject: Schedule of Meeting on Monday(03.12.2018)

Sat, Dec 1, 2018 at 11:00 AM

From: pramodhini r <pramodhini11@gmail.com>
To: vinaykumarc5891@gmail.com

Print please. Hod wants it

Forwarded message
From: Varsha Prasad <varsha.prasad@nmit.ac.in>
Date: Sat, 1 Dec 2018, 10:43
Subject: Fwd: Schedule of Meeting on Monday(03.12.2018)
To: pramodhini r <pramodhini11@gmail.com>

Forwarded message
From: Varsha Prasad <varsha.prasad@nmit.ac.in>
Date: Fri 30 Nov, 2018, 3:40 PM
Subject: Schedule of Meeting on Monday(03.12.2018)
To: Dr.Sandya S <sandya.prasad@nmit.ac.in>
Cc: <deebalakshmi.gr@nmit.ac.in>

Respected mam,

As per your suggestion meeting is scheduled in RnD Lab from 10:30 am onward to discuss the syllabus of the current semester subjects. Please find the schedule.

Sl No	Timing	Subjects	Faculty Members	Agenda
1	10:30am -10:45am	DSP	Dr Raghunandan Dr Prashanth H S	Inclusion of DSP architecture in DSP syllabus (4 th sem-2017-21 scheme)
2	10:45am -11:00am	DIP	Dr Prashanth H S Dr Raghunandan	DIP to be offered as elective for 6 th sem-2014-18 scheme. Syllabus content to be discussed.
3	11:00am-11:15 am	Machine Learning for Pattern Recognition	Dr Raghunandan Dr Jayavrinda V	ML to be offered as elective for 6 th sem-2014-18 scheme. Syllabus content to be discussed.
4	11:30am-12:00 pm	DSD using Verilog	Mr. Shashidhar Ms Manjula B M Ms Rekha Padke	DSD using Verilog syllabus discussion. Lab software/hardware requirement details Lab Manual
5	12:00 -12:30pm	Advanced Microcontroller	Prof. Shankar Prof. Yaji Ms Divya	Advanced Microcontroller syllabus discussion. Lab software/hardware requirement details Lab Manual
6	12:30pm	SDR	Mr Anandthreetha	SDR to be offered as elective for 6 th sem-2014-18 scheme. Syllabus content to be discussed.

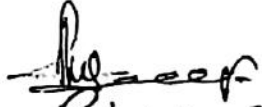
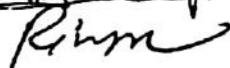
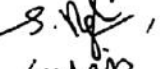
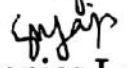
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CIRCULAR

Date-28-04-2018


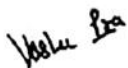
As per Internal BoS meeting held on 28-4-2018, discuss on scheme and syllabus by the following reviewers will be held on Monday 30-4-2018. The Schedule is enclosed. All the faculty members need to mandatory attend the meeting and finalize the scheme and syllabus for 2017-21 batch.

Reviewers:

- | | | | |
|------------------------|---|------------------------|--|
| 1. Prof. Mahavir Swamy | - | R&D Lab. |  |
| 2. Dr. S L Pinjare | - | Project Lab. |  |
| 3. Dr. Raghunandan | - | DCN Lab. |  |
| 4. Prof. Sitaram Yaji | - | Digital Lab. |  |
| 5. Prof. Sankar Dasiga | - | Power Electronics Lab. | |



The faculty members need to bring the modified syllabus for the meeting. Please refer VTU syllabus for modification.

BOS coordinators


28/4/2018
HOD, ECE

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Nelabanka
Bangalore - 560 064

	Department of Electronics and Communication Engineering			
TITLE: Minutes of UG Internal BoS Meeting	DESCRIPTION: Minutes of UG internal BoS Meeting	Year: 2017- 2018	Time: 10:45 AM to 1:15 PM	Date: 05/FEB/18 and 06/FEB/18

The Internal BoS Meeting was scheduled on 05/02/18 and 06/02/18 to discuss the scheme and syllabus for 2017-2021 batch. This is in requirement to address the placement needs and to incorporate recent development in each domain. As Placement questions stress the need for domain knowledge on networking, ARM controller, OS Fundamental's, Artificial Intelligence, 4G LTE and Scripting Language. The scheme and syllabus was scrutinized and the following changes in the scheme and syllabus were suggested.

III and IV Semester

- There is no change in AEC, DE, NA and Maths of 3rd sem scheme.
- There is no change in LIC, DSD Using VL, CS and Maths for 4th sem scheme.
- The contents of each of the subject of 3rd and 4th sem must be revisited by the allotted subject teachers in consultation with the subject expert.
- Signals and Systems is to be moved to 4th Sem and Field Theory to 3rd Sem.
- Credits allotted for the subject Microprocessor and Microcontroller (3rd sem) is to be rechecked.
- For Microprocessor and Microcontroller (3rd sem), teaching hours can be allotted as 3+1 (3 hrs for theory+ 1hr for lab). The syllabus should comprise of 1 unit of 8086 processor and 4 units of 8051 controller. *subject title to rename.*
- In 4th Sem Microcontroller subject syllabus needs to be reframed. The syllabus should include ARM Cortex M3.
- The Microcontroller Lab (4th sem) should include simulation and interfacing experiments using ARM M3.
- In Control Systems and Signals and Systems tool centric assignments using Matlab is to be included.
- In AEC lab (3rd Sem) simulation experiments.

Action ITEM: Each subject teachers

Subject teachers & Experts list enclosed.

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V and VI Semester

- There is no change in DSP, AC, MW, F.VLSI and DS using C++ of 5th sem scheme.
- There is no change in DC, ANT and OR for 6th sem scheme.
- The contents of each of the subject of 5th and 6th sem must be revisited by the allotted subject teachers in consultation with the subject expert.
- Microwave subject must include devices and TWT.
- Computer Communication Networks which was in 7th Semester will be shifted to 6th Semester.
- Information Theory and Coding from 6th Semester will be moved to 7th Semester.
- Scripting Language (Python) is to be introduced as core elective in 5th Semester.
- ESSD is removed from 5th sem core elective.
- IOT is ~~removed~~ ^{added in} 7th sem core elective.
- It is yet to be decided whether MEMS (Core Elective) can be shifted to 6th semester.
- Fundamentals of Operating Systems is to be introduced as core elective in 6th Semester.
- The credits allotted for Operation Research is to be revisited.
- There is no change in 6th sem open electives.
- Subjects can be introduced as Core/Open electives based on need.

Action ITEM: Each subject teachers

VII and VIII Semester

- There is no change in OFC, ENT and PE of 7th sem scheme.
- There is no change in WC of 8th sem scheme.
- The contents of each of the subject of 7th and 8th sem must be revisited by the allotted subject teachers in consultation with the subject expert.
- ITC must include one unit of ~~ECC~~.
- AI/Machine Learning is to be introduced as core elective in 7th Semester.
- Sensors and Actuators and ANN is removed from 7th sem Open Elective.
- SOC Design Using FPGA, Advanced DSP and ~~ANN~~ ^{ANN} is to be introduced as core elective in 7th Semester.
- Cryptography of 8th sem core elective must include contents on Steganography/ Ethical Hacking.
- 4G LTE ~~is~~ ^{to be} introduced as a core elective in 8th sem.
- WSN ~~is~~ ^{to be} introduced as a core elective in 8th sem.
- Subjects can be introduced as Core/Open electives based on need.

Action ITEM: Each subject teachers

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NOTE:

- The prescribed textbook for the subjects must be revisited.
- Text Book used by the subject teacher needs to be clearly indicted in the syllabus. Subject teachers should use the same textbook for setting the MSE Question Papers & teaching
- Reference book to be included in the syllabus.
- CO/POs of all subjects must be revisited and Blooms Taxonomy should be considered.

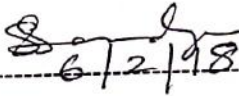
Action ITEM: Each subject teachers

BoS Coordinators

Vasha Poasadi

Sowmya J

Pramodhini-R



6/2/18

Chairperson of BoS, ECE, NMIT
and Head of Department, ECE, NMIT

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

BOARD OF STUDIES**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

2017-18

Date:12/05/17

Date of BoS meeting	9 th MAY 2017	Expertise
MEMBERS		
External	1) Dr.Rathna G.N,IISC	Communication and signal Processing
	2) Dr.Ravish Aradhya, Prof,RVCE	VLSI Design and Embedded systems
Student alumni	1) Ms.Pruthvi, OSI energy Automation LTD	Embedded systems
	2) Mr.Anandtheerth. S. Mathad, NMIT	Communication
Chairman	Dr. Sandya S, HoD, Dept ECE	Communication and Embedded Systems
internal	1) Dr. S.L Pinjare	VLSI

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Department of Electronics & Communication Engg
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Bangalore - 560 064

	2) Dr.Raghunandan	Communication
	3) Prof. Sankar Dasiga	Embedded Systems
	4) Dr.Rukmini	Communication
	5) Dr.Veda Nagraj	VLSI, MEMS
	6) Prof. MahaviraSwamy N	Communication

Dr.Sandya S welcomed all the BoS members.

Agenda of the Board of Studies meeting 2017-18

1. Approval of scheme and syllabus for UG VII-VIII sem 2014-18 batch
2. Approval of syllabus of Basic Electronics for the 2017-2021 batch
3. Approval of scheme and syllabus for PG programs
 - i) VLSI Design and Embedded system
 - ii) Digital Communication and Networking

Head,
 Department of Electronics & Communication Engg
 Nitte Meenakshi Institute of Technology
 Govindapura, Yelahanka
 Bangalore - 560 064

Minutes of BoS meeting –PG Digital Communication and Networking

1. Dr Ravish Aradhya H.V and Dr Rathna raised concerns that there was no core subject on networking being offered in 1st Sem of DCN. It was suggested to move **Advanced Embedded System** to Elective group and offer **Advanced Computer Networks** as a core subject.

Action: Inputs Shall be considered and will be implemented for 2018-2020 batch

2. Members of the BOS suggested that **RF and Microwave** which is currently in 2nd Sem can be moved to 1st Sem and **Antenna Theory and Design** to 2nd Sem.

Action: Inputs Shall be considered and will be implemented for 2018-2020 batch

3. Anandtheerth –Alumini- PG, DCN suggested to introduce a subject on Simulation, Modelling and Analysis as an elective.

Action: Inputs shall be considered and will be discussed in DPGC

4. Members of the BOS were of the opinion that, the electives is to be re-arranged under two separate groups, namely **Communication and Networking**.

Action: Corrections shall be made

5. Dr Rathna suggested to introduce new subjects such as **Wireless Sensor Network, SDN, SDR** in 3rd Sem as Self Study Component, where during the first two weeks the faculty can give an introduction to the subject and in the remaining weeks on every Saturday the students can present papers from leading publishers on that subject.

Action: Inputs shall be considered and discussed in DPGC

6. Members of the BOS suggested that, Unit 4 and 5 of **Advanced Mathematics** is to be changed, and application specific topics such as **Random Process, Probability** etc. is to be included.

Action: Input Shall be considered and discussed in DPGC

7. Dr Ravish and Dr Rathna suggested that students **term project** shall be rolled out as a papers

Action:Inputs shall be considered

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8. Dr Rathna suggested including topics on CNN in Artificial Neural Networks syllabus. And Artificial Neural Networks can be made common subject for both VLSI and DCN stream.

Action: Inputs Shall be considered and discussed in DPGC

9. For RF and Microwave subject, it was suggested to reorganize the contents, include double stub application, avoid overlapping with UG 5th Sem Microwave syllabus and to include Text 2 in reference and not as Text Book.

Action: Inputs are considered and corrections are made


12/5/17
HoD, ECE

(Dr.Sandya S)

Head,
Electronics & Communication Engg
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Minutes of BoS meeting –PG VLSI Design and Embedded Systems

1. Dr Ravish Aradhya and Dr Rathna suggested that students **term project** shall be rolled out as a paper

Action: Inputs shall be considered

2. The **Advanced Mathematics** subject content is to be revisited for VLSI stream.

Action: Shall be discussed in DPGC

3. Dr Ravish Aradhya suggested that a subject on **Static Timing Analysis** is to be introduced in 1st Sem.

Action: Inputs shall be considered and implemented for 2018-2020 batch

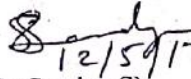
4. Dr Ravish Aradhya suggested introducing new elective subjects such as **SOC, Embedded Networking** and **VLSI Testing & Verification** for 3rd Sem.

Action: Inputs shall be considered and discussed in DPGC

5. For **Low Power VLSI Design** it was suggested to retain **Adiabatic Circuits** in the Syllabus.

Action: Inputs are considered and under execution

HoD, ECE


12/5/17
(Dr. Sandya S)

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bengaluru - 560 064

MINUTES OF Board of Studies MEETING -UG

1. Dr.Ravish Aradhya H.V suggested that 'Miniproject' of 2 credits after 6th Semester can be renamed as 'Minor project' and it may or may not be continuation of the final year major project.

Action: Inputs shall be considered and shall be taken up in Academic council meeting

2. He also suggested to revise the elective names as follows:

- Core electives as A,B,C and so on
- Open electives as 1,2,3 and so on

Action: Inputs considered and implemented

3. It was suggested that Artificial Neural Network to be moved into Core Elective group for 7th Sem.

Action: Inputs shall be considered and will be discussed in DUGC meeting

4. Dr Rathna suggested that Stegography can be included in Cryptography course in 8th Sem.

Action: Shall be considered and will be discussed in DUGC meeting

5. Dr Ravish Aradhya suggested that the course on FPGA Architecture to be made lab centric and the process of evaluation should be reviewed.

Action: The inputs given are under Execution

6. In case the same subject is offered as open elective and core elective , the contents of core elective must have a more detailed syllabus.

Action: The inputs given are under Execution

7. Dr Rathna raised concerns on offering **Random Process** as a Open Elective as CSE/ISE students would have studied the same concepts in Maths. In case ,even if its offered the syllabus needs to be framed taking into consideration the Mathematics subject, to minimize overlapping.

Action: Inputs shall be considered

8. Syllabus for Basic Electronics should be common for all branches of Engineering

9. Reorganise units of Basic Electronics contents for equal distribution of number of hours as:

- i) It was suggested to move amplifiers component from unit4 to unit3

Action: Inputs considered and implemented

Head,
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Nitte Meenakshi Institute of Technology
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Bangalore - 560 064

NTTE MEENAKSHI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Date: 08/05/2017

UG and PG BoS meeting for the year 2017-18

PANEL MEMBERS

Date:	09 th MAY 2017
Members	
External	1. Dr. Rathna Principal Research Scientist, IISC Blore <i>Rathna. G. N.</i> 2. Dr. Ravish Aradhya H.V, RVCE, Blore <i>Ras</i> 9/5/17 3. Ms. Pruthvi, Alumni, NMIT <i>Pruthvi</i> 9/5/17 4. Mr. Anandteerth S Mathad, Alumni, NMIT <i>A. S. Mathad</i>
Internals	1) Dr. Sandya S <i>Sandya S</i> 9/5/17 2) Prof Sankar Dasiga <i>Sankar Dasiga</i> 9/5/2017 3) Dr. S.L Pinjare <i>S.L Pinjare</i> 9/5/2017 4) Prof. Mahavira Swamy <i>Mahavira Swamy</i> 9/5/2017 5) Dr. Raghunandan <i>Raghunandan</i> 9/5/17 6) Dr. Veda <i>Veda</i> 9/5/17

HoD, ECE

Sandya S
8/5/17
(Dr. Sandya S)

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

BOARD OF STUDIES**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING****2017-18****Date:12/05/17**

Date of BoS meeting	9 th MAY 2017	Expertise
MEMBERS		
External	1) Dr.Rathna G.N,IISC	Communication and signal Processing
	2) Dr.Ravish Aradhya, Prof,RVCE	VLSI Design and Embedded systems
Student alumni	1) Ms.Pruthvi, OSI energy Automation LTD	Embedded systems
	2) Mr.Anandtheerth. S. Mathad, NMIT	Communication
Chairman	Dr. Sandya S, HoD, Dept ECE	Communication and Embedded Systems
internal	1) Dr. S.L Pinjare	VLSI

Head,
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Govindapura, Yelahanka
Bangalore - 560 064

	2) Dr.Raghunandan	Communication
	3) Prof. Sankar Dasiga	Embedded Systems
	4) Dr.Rukmini	Communication
	5) Dr.Veda Nagraj	VLSI, MEMS
	6) Prof. MahaviraSwamy N	Communication

Dr.Sandya S welcomed all the BoS members.

Agenda of the Board of Studies meeting 2017-18

1. Approval of scheme and syllabus for UG VII-VIII sem 2014-18 batch
2. Approval of syllabus of Basic Electronics for the 2017-2021 batch
3. Approval of scheme and syllabus for PG programs
 - i) VLSI Design and Embedded system
 - ii) Digital Communication and Networking

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Chandapura, Mysuru
Bangalore - 560 064

MINUTES OF Board of Studies MEETING -UG

1. Dr.Ravish Aradhya H.V suggested that 'Miniproject' of 2 credits after 6th Semester can be renamed as 'Minor project' and it may or may not be continuation of the final year major project.
Action: Inputs shall be considered and shall be taken up in Academic council meeting
2. He also suggested to revise the elective names as follows:
 - Core electives as A,B,C and so on
 - Open electives as 1,2,3 and so onAction: Inputs considered and implemented
3. It was suggested that Artificial Neural Network to be moved into Core Elective group for 7th Sem.
Action: Inputs shall be considered and will be discussed in DUGC meeting
4. Dr Rathna suggested that Stegnography can be included in Cryptography course in 8th Sem.
Action: Shall be considered and will be discussed in DUGC meeting
5. Dr Ravish Aradhya suggested that the course on FPGA Architecture to be made lab centric and the process of evaluation should be reviewed.
Action: The inputs given are under Execution
6. In case the same subject is offered as open elective and core elective , the contents of core elective must have a more detailed syllabus.
Action: The inputs given are under Execution
7. Dr Rathna raised concerns on offering Random Process as a Open Elective as CSE/ISE students would have studied the same concepts in Maths. In case ,even if its offered the syllabus needs to be framed taking into consideration the Mathematics subject, to minimize overlapping.
Action: Inputs shall be considered
8. Syllabus for Basic Electronics should be common for all branches of Engineering
9. Reorganise units of Basic Electronics contents for equal distribution of number of hours as:
 - i) It was suggested to move amplifiers component from unit4 to unit3
Action: Inputs considered and implemented

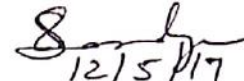
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ii) Dr S.L Pinjare suggested to include Biasing schemes such as voltage divider biasing in unit3 amplifier component.

Action: Inputs cannot be considered since we are addressing both circuit and non circuit branches.

iii) Dc load concept for diode is to be included in unit2.

Action: Inputs considered and implemented


12/5/17
HoD, ECE

(Dr.Sandya S)

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ACADEMIC YEAR: 2017-2018 (May)

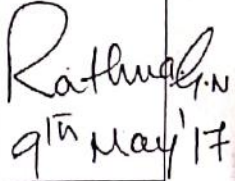
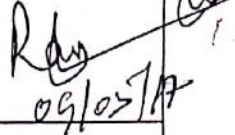
SI No.	NAME	DESIGNATION	AFFILIATION	MEMBER	DOMAIN
1	Dr Sandya S	Professor and Head, BOE Chairman	NMIT, Bangalore	Internal	Satellite Communication , Embedded Systems, SDR, Fault Tolerant System Design
2	Dr.Shankarananda			VTU Nominee	
3	Dr Rathna	Principal Research Scientist	IISc, Bangalore	External	Image Processing, Real Time Signal processing, Sensor Networks
4	Dr Ravish Aradhya H V	Professor	NMIT, Bangalore	External	VLSI and Embedded Systems
5	Ms Pruthvi	Software Engineer	OSI energy Automation LTD	Alumni Member	Automotive Electronics
6	Mr Anandteerth S Malnad	Assistant Professor	NMIT, Bangalore	Alumni Member	SDR, Communication
7	Dr S L Pinjare	Professor	NMIT, Bangalore	Internal	VLSI, MEMS
8	Dr Raghunandan	Professor	NMIT, Bangalore	Internal	Machine Learning, IOT, Image and Signal processing
9	Dr Rukmini	Professor	NMIT, Bangalore	Internal	Antenna and Wireless Communication
10	Prof. MahaviraSwamy	Professor	NMIT, Bangalore	Internal	Wireless /Satellite Communication
11	Prof. SankarDasiga	Professor	NMIT, Bangalore	Internal	Automotive Electronics, IOT
12	Dr Veda	Assoc. Professor	NMIT, Bangalore	Internal	MEMS

Head,
Department of Electronics & Communication Engg.
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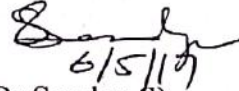
NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

External BoS members

Date: 06/05/2016

Sl no	Name member	Organization	Area of interest	Email id	Signature
1	Dr.Rathna G.N	IISC	DSPProcessors, Embedded systems	rathna@ee.iisc.ernet.in	 9 th May '17
2	Dr.Ravish Aradhya H.V	RVCE	VLSI	ravisharadhya@rvce.edu.in	 09/05/17
3	Dr.Purushothaman Surendran	KPIT	Embedded Systems	purushothman.surendran@kpit.com	

HoD, ECE




6/5/17
(Dr.Sandya S)

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

ACADEMIC YEAR: 2016-2017(MAY)

SI No	NAME	DESIGNATION	AFFLIATION	MEMBER	DOMAIN
1	Dr Sandya S	Professor and Head, BOE Chairman	NMIT, Bangalore	Internal	Satellite Communication, Embedded Systems, SDR, Fault Tolerant System Design
2	Dr.Shankarananda			VTU Nominee	
3	Dr Rathna	Principal Research Scientist	IISc, Bangalore	External	Image and Signal processing
4	Dr N C Shivaprakash	Chief Research Scientist	IISc, Bangalore	External	Instrumentation , Applied Physics
5	Mr Purushothaman	Senior Technical Lead	KPIT, Bangalore	External	Automotive Electronics
6	Mr Shomashekar	Co-Founder and CEO	Analog Semiconductors, Bangalore	External	Analog VLSI
7	Mr. Vishal Mackton	Software Engineer	HP, Bangalore	Alumni Nominee	Software Engineering
8	Dr K N Haribhat	Professor	NMIT, Bangalore	Internal	Cryptography, Error Control Coding
7	Dr Prashanta H S	Professor	NMIT, Bangalore	Internal	Image and Signal processing
8	Dr Sreenivasappa	Professor	NMIT, Bangalore	Internal	Power Electronics
9	Prof. SankarDasiga	Professor	NMIT, Bangalore	Internal	Automotive Electronics, IOT
10	Prof.MahaviraSwamy	Professor	NMIT, Bangalore	Internal	Wireless /Satellite Communication
11	Prof.SitaramYaji	Professor	NMIT, Bangalore	Internal	IOT, Networking
12	Mr Rajesh N	Assoc. Professor	NMIT, Bangalore	Internal	Image and Signal processing
13	Mr Shashidhar	Assoc. Professor	NMIT, Bangalore	Internal	FPGA, Digital System Design using HDL

Head,
Department of Electronics & Communication Engg.
Nitte Meghakshi Institute of Technology
 Govindapura, Yelahanka
 Bangalore - 560 064

	Department of Electronics and Communication Engineering			
TITLE: Minutes of PG BoS Meeting	DESCRIPTION: Minutes of BoS Meeting for two streams of M.Tech Program – VLSI & Embedded Systems and Digital Communication Networks	Year: 2016	Time: 9:30PM – 12:30PM	Date: 01/Oct/16

Participants		
External	Internal	Alumni
1. Dr Shiva Prakash (IISc) 2. Dr Rathna (IISc) 3. Dr TV Prabhakar (IISc) 4. Dr Bharadwaj Amrutur (IISc) 5. Dr Manjunatha Hebbar (Buoyanci) 6. Dr Somasekhar (Analog Semi) 7. Dr Purushoththaman (KPIT)	1. Prof RanganathaSetty 2. Prof HC Nagaraj 3. Prof Sandya 4. Prof Hari Bhat 5. Prof Prashanth 6. Prof SL Pinjare 7. Prof Padmavathi 8. Prof SankarDasiga 9. Prof Veda Nagaraj 10. Prof Raghunandan 11. Prof. Girish G K 12. Ms.Sowmya.J	1. Rashmi Kulkarni 2. Kannan 3. Arun Kumar

Proceedings

Comments from	Comments
Dr Sandya	- Introduced Vision and Mission of ECE Dept VLSI & ESScheme and Syllabus review
Dr Shiva Prakash	<ul style="list-style-type: none"> - Vision of NMIT and ECE should be consistent - NBA accreditation – “Extended”, not “renewed” - Include TEQIP in list in slide on Strengths - Change teaching hours for some courses from 4 hrs / week to 3 hrs / week and include some tutorials - “Mini project” should be renamed – let it be consistent with final Project ... call them Project Phase 1,2,3, ... - 100 credits is too much, nowadays even 64-70 is ok - Prefix of “Advanced” in some course-titles – what is Advanced? Avoid this - VLSI or ES – which is more important? - Build a strong common foundation for both ES and VLSI, and teach in first semester
Dr Bharadwaj	<ul style="list-style-type: none"> - Common foundation must emphasize on ES - More industry people want ES and only very few companies want VLSI - ES goes hand-in-hand with Basic Electronics – teach in Foundation
Dr Somasekhar	- Do you want to be niche (VLSI) or common (ES)?
Dr Hebbar	- Electronics Systems Design is needed
Dr Bharadwaj	- SW skills are critical; Basic C and Data structures are important

Head,
 Department of Electronics & Communication Engg.
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Dr Purushotthaman	<ul style="list-style-type: none"> - Project plays an important role - Critical mass needed – can't do much for a small strength
Dr Bharadwaj, Dr Shiva Prakash	<ul style="list-style-type: none"> - Reduce lecture hours, introduce more labs / tutorials - Should not have electives in first semester
Dr Rathna	<ul style="list-style-type: none"> - Should not have pre-requisites for any course in first semester
Dr Purushotthaman	<ul style="list-style-type: none"> - More MNCs want ES than VLSI
Dr Shiva Prakash	<ul style="list-style-type: none"> - What are the basic foundation courses (needed for both ES and VLSI, and which you should offer in first semester)?
Dr Purushotthaman	<ul style="list-style-type: none"> - More ES companies; so teach ES more in foundation / first semester
Dr Bharadwaj	<ul style="list-style-type: none"> - Yes, ES is needed for even Satellite research and Robotics research
Dr Somasekhar	<ul style="list-style-type: none"> - Where is uniqueness? Result: VLSI has severe shortage
Dr Shiva Prakash	<ul style="list-style-type: none"> - Can we change titles of courses? <ul style="list-style-type: none"> o Response from Prof Veda: No.
Dr Prabhakar	<ul style="list-style-type: none"> - Students should take online courses and these can be augmented by offline classes by teachers, who have taken up those courses themselves
Dr Bharadwaj, Dr Prabhakar	<ul style="list-style-type: none"> - Enable industry people to come and teach full courses / semesters
Dr Sandya	<ul style="list-style-type: none"> - Like IEEE e-blended programs
Dr Bharadwaj	<ul style="list-style-type: none"> - ES: Need FPGA to be taught. SCL gives facilities free for Academic institutions
Dr Somasekhar	<ul style="list-style-type: none"> - Semesters 1,2 & 3,4 have some imbalance, in terms of contact-hours versus credits - Suggestion: change number of credits in semesters as 26,26,24,24
Dr Rathna	<ul style="list-style-type: none"> - Rename mini-project as term-project - Foundation courses should not have pre-requisites; if you need students to know something, tell them and they should study, but don't write explicitly
Dr Bharadwaj Dr Shiva Prakash	<ul style="list-style-type: none"> - Maths syllabus – it is UG level, why repeat? What you need are things like Signals and Systems, Transforms, etc. - Need topics like scripting, automation, etc. as foundation courses
Dr Somasekhar	<ul style="list-style-type: none"> - Include things like Perl, Tcl/tk in foundation courses
Dr Shiva Prakash	<ul style="list-style-type: none"> - Math course to be revamped - Cover basics in Unit 1 in every course
Dr Purushotthaman	<ul style="list-style-type: none"> - ES: Real-time systems, RTOS, basic Embedded programming / Embedded Linux – needed to be taught for foundations in ES
Dr Somasekhar	<ul style="list-style-type: none"> - Can you separate VLSI and ES as two different M.Tech programs? - Change title of AES course
Dr Purushotthaman	<ul style="list-style-type: none"> - Suggestion for ES <ul style="list-style-type: none"> o Sem 1: Intro to ES, Emb Linux, etc o Sem 2: VxWorks, etc.
Dr Prabhakar	<ul style="list-style-type: none"> - Include in ES: Microcontrollers, Sensors, Actuators, Power supply, need Embedded System Design, I²C, separate HW and SW courses, ..
Dr Somasekhar	<ul style="list-style-type: none"> - Ref CMOS VLSI Design course – talk about non-VLSI also in Unit 1
Dr Bharadwaj	<ul style="list-style-type: none"> - Teach few things but teach very well - Class hours should be for fundamentals
DCN Scheme and Syllabus review	
Dr Shiva Prakash	<ul style="list-style-type: none"> - Don't use "Advanced" as prefix in course titles
Dr Rathna Dr Prabhakar	<ul style="list-style-type: none"> - Tune Maths for each stream
Dr Shiva Prakash	<ul style="list-style-type: none"> - Networking is needed as "core", not only as elective

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Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Gowdohpetta, Yelabanka
Bangalore - 560 064

Dr Purushotthaman	- Change from Adv Computer NW to Adv Communication NW
Dr Prabhakar	- Teach NM1, NM2, MAC, ARQ, etc..... layer-wise ... Stop/Wait, Deep Learning, etc
Dr Shiva Prakash	- Teach machine learning
Dr Shiva Prakash Dr Purushotthaman	- Can you change from "VLSI & ES" and "DCN" to "VLSI" and "ES & DCN"? - Phase out some courses and Phase in some other courses
Dr Shiva Prakash	- You can have Signal processing as elective and NW Programming as core
Dr Purushotthaman	- We at KPIT re-teach same things after your students join us - Teaching needs to be strong - Try online courses – blend
Dr Bharadwaj	- Try open-book exams for better results
Dr Hebbar	- You have your research programs which are long-lasting. Based on those, you can design courses which will feed into / consistent with them.

Post the BoS meeting, there was a discussion between the HoD and the Director and Principal. It was decided to consider balancing the proportions of VLSI and ES components in the corresponding program.

Action items

#	Action item	Status / Remarks
1	VLSI versus ES – what is our emphasis? What do we want to be? 50-50? Different? Review course structure from the point-of-view of this decision.	
2	Identify "Foundation courses" – common for VLSI & ES	
3	Can we re-structure to offer all Foundation courses in First semester?	
4	Change titles (Example: to remove pre-fix "Advanced")	
5	Math course (now at UG level) to be revamped – and customize to streams. If this is not done, Math to be removed as mandatory course..?	
6	Consider reducing lecture hours and increasing lab hours or introducing tutorial sessions	
7	Pre-requisites not to be mentioned in first semester. They need to be covered by students studying themselves or in first Unit by teacher	


4/10/16

Chairperson of BoS, ECE, NMIT
and Head of Department, ECE, NMIT

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

BOARD OF STUDIES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Date: 17/05/16

Date	14MAY 2016
MEMBERS	
External	Dr.Ratna,IISC Dr.ShivaPrakash,IISC Dr.Somashekar B, Analog semiconductors Dr.Purushothaman, KPIT
Chairman	Dr.Sandya S, HoD, Dept ECE
Internal	Dr.HariBhat,Dr.Prashantha, Prof Sankar Dasiga,Prof Sitaram Yaji, Prof MahaviraSwamy,MrRajesh,Mr.Shashidhara

1. Dr. Sandya S welcomed all the members.
2. Dr.Sandya S presented the proposed scheme and syllabus for V-VIII semester for the 2014-2018 batch

MINUTES OF THE MEETING

1. Relatively more subjects (at least 5 subjects) to be offered to the students to opt as an elective.
2. An orientation program to be organised for the students to create awareness about choosing the right elective as per the student's interest.
3. The core elective subjects to be subsets of the either embedded systems, signal processing, VLSI, communication, etc so that the students can be specialised in a particular domain
4. Link of the subjects across core electives to be shared to students so as to plan their domain
5. While the subjects are streamlined in a particular order, it gives clarity for the recruiters during the recruitment drives for selecting a student who has been streamlined in a particular domain.
6. The syllabus of the offered electives to be fine tuned as per the industry requirement
7. The open elective subjects to be offered in such a way that the other department (IS, CS, EEE, Civil, Aero) students can opt the subject provided the students of the offering department should not be permitted to opt the same.
8. The open elective offered to other departments should be at the basic level such that even a student with 10+2 knowledge can take up the elective.
9. The open elective which is offered at the elementary level to be without any pre-requisites

Head,
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Govindapura, Yelahanka
Bangalore - 560 064

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NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

BOARD OF STUDIES Year-2016


PANEL MEMBERS

Date of BoS meet	14 th MAY 2016
Members	
External	1. Dr. Rathna C.N Principal Research Scientist, IISC, Blore 2. Dr. N.C Shiva Prakash, Chief Research Scientist, IISC, Blore 3. Mr. Purushothuman, KRIT 4. Mr. Somashekar, Analog semiconductors
Internals	1) Dr. Sandya S 2) Dr. Prasanth H.S 3) Prof. Sankar Dasiga 4) Dr. Sreenivasappa 5) Dr. Hari Bhat 6) Prof. Mahavira Swamy 7) Prof. Sitaram Yaji 8) Mr. Rajesh 9) Mr. Shashidhar

Time: 9.00 am

Venue: R & D lab

HoD, ECE


19/5/16
(Dr. Sandya S)

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Gowdopura, Yelahanka
Bangalore - 560 004

1

Department of Electronics and Communication Engineering

CIRCULAR

Date: 21/01/2015

The DUGC members are required to attend the meeting to be held on 23/01/2015 (Friday) in the department to approve the syllabus of **Autonomy** **electronics** offered as core elective to the final year students of ECE and EEE Dept.

Following are the DUGC members

SL NO	NAME OF THE FACULTY	DESIGNATION
1.	Dr.S.Sandya	Chairperson
2.	Dr.Prashanth	Member
3.	Mr. Sankar Dasiga	Member
4.	Ms.Soumya .M	Member
5.	Ms.Shylaja	Member

Venue: R&D lab

Time: 10.30.A.M


HoD, ECE 27/01/15

(Dr.Sandya. S)

Head,

Department of Electronics & Communication Engg
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

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Department of Electronics and Communication Engineering

CIRCULAR

Date: 27/01/2015

A DUGC meeting was held on 23/01/2015 for the approval of syllabus of ~~Automotive Electronics~~ offered as core elective for final year students of ECE and EEE Dept.

Following members were present

SL NO	NAME OF THE FACULTY	DESIGNATION	Signature
1.	Dr.S.Sandya	Chairperson	
2.	Dr.Prashanth	Member	
3.	Prof. Sankar Dasiga	Member	
4.	Ms.Soumya .M	Member	
5.	Ms.Shylaja	Member	

Following points were discussed

- 1) Prof. Sankar Dasiga (course coordinator) and Ms. Shylaja (faculty for the course) prepared a draft document with Prerequisites, Syllabus, COs, Evaluation Methodology etc
- 2) The draft syllabus was discussed and approved
- 3) The draft prerequisites for the course were discussed and inclusions: a) inclusion of basic C programming skills, b) Knowledge of basics of Matlab and simulink, were suggested
- 4) It was discussed and finalized that
 - a. For the current final year ECE and EEE streams, towards addressing the requirements of KPIT per the MoU and also reamping up the students for employment opportunities in the areas of Automotive Electronics & Infotainment, an open elective titled "Automotive Electronics" would be offered in the 8th semester and a special certificate course on "Autosar" would be conducted during the forthcoming summer break

Head,
Department of Electronics & Communication Engg
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

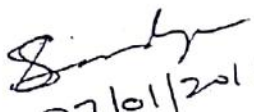
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- b. For the current 3rd year students, an option to attend the special certificate course on "Autosar" during the forthcoming summer break and, an open elective on "Automotive Electronics" in the 7th semester would be offered
- c. For the current 2nd year students and also going forward electives – "Automotive Electronics" and "Autosar" would be offered in the 6th and 7th semesters respectively

Additional Points:

- Mini projects based on Matlab/Simulink to be considered for assignments
- A proposal to be prepared by Ms.Shylaja to setup a lab for Automotive Electronics
- A seminar on "Automotive Electronics" would be organized on Feb 7th, 2015
- Ms.Chaitra to attend Automotive electronics classes after CIE-1

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27/01/2015
Head,
Department of Electronics & Communication Engg
Nitte Meevakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

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Department of Electronics and Communication Engineering

CIRCULAR

Date: 27/01/2015

A DUGC meeting was held on 23/01/2015 for the approval of syllabus of Automotive Electronics offered as core elective for final year students of ECE and EEE Dept.

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SL NO	NAME OF THE FACULTY	DESIGNATION	Signature
1.	Dr.S.Sandya	Chairperson	
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Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

BoS Meeting

Date: 17/04/15

The BoS meeting for the academic year 2015 was held in the department of Electronics and Communication Engg on 17/04/15 for the approval of scheme and syllabus of III and IV semester.

Following external members were present

Dr.Rathna C.N, Principal Research Scientist,IISC Blore.

Following external members were present

- 1) Dr.Sandya S
- 2) Dr.Prasahantha H.S
- 3) Prof Sankar Dasiga
- 4) Dr.Sreenivasappa
- 5) Dr.HariBhat
- 6) Prof.MahaviraSwamy
- 7) Ms.Veda
- 8) Ms.Manjula
- 9) Ms.Naina
- 10) Mr.Shashidhar
- 11) Ms.Rekha Phadke

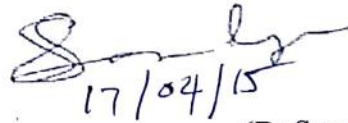
The following points were discussed.

1. The total no. of hours (i.e., L-T-P) has to be changed accordingly for each subject
2. To add more headings / contents at the beginning of each unit
3. The pre-requisites and CO-PO mapping has to be revisited
4. The sub sections such as 1.1, 1.11 etc. not to be specified
5. Make sure that we have at the maximum of 1 or 2 text books for each subjects
6. To ensure that whether the sequence is maintained in the contents of the syllabus flow
7. Compare to **Basic Electronics** and correlate syllabus of **Analog Electronic Circuits** theory and Lab and the text book Millman to be removed from theory
8. Prescribe latest edition of Roy Choudhary text book for Network Analysis .In Unit 5 Transient Response to be included which is chapter 15 in Roy Choudhary, also to decide whether the skipped chapters 4 and 7 of Roy choudhary to be included in syllabus
9. In **Digital Electronics** theory rearrange the contents of Unit 4 and 5, such that one text book can address the requirements completely with appropriate distribution of teaching hours.

Head,
Department of Electronics & Communication Engg.
Nitte Meechakshi Institute of Technology
Gowdappur, Yelahanka
Bangalore - 560094

10. **Fields and Waves** to be retained in IV semester
11. In **Microcontroller -I** , ensure that each unit content is adequate for 9 hrs. of distribution so that 20 marks question from each is feasible to be given
12. Unit 1's of MC-1 and MC-2 may be swapped
13. Update the list of experiments to have an overall no as 9 by clubbing few experiments as Part A and B as one experiment
14. Add an experiment to have transistor characteristics in **AEC lab**
15. **MC LAB -I** , be specific about which experiment to be done in assembly language AND using C , also be specific which experiment are to be done using 8051 and which with MSP430

HoD,ECE



17/04/15

(Dr.Sandya S)

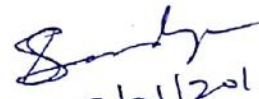
Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Gowdangudi, Mysuru
Karnataka

- b. For the current 3rd year students, an option to attend the special certificate course on “Autosar” during the forthcoming summer break and, an open elective on “Automotive Electronics” in the 7th semester would be offered
- c. For the current 2nd year students and also going forward electives – “Automotive Electronics” and “Autosar” would be offered in the 6th and 7th semesters respectively

Additional Points:

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--##--


27/01/2015

Head,
Department of Electronics & Communication Engg.
Nitte Meghadesh Institute of Technology
Gowdabasara, Yelahanka
Bangalore - 560 069

Department of Electronics and Communication Engineering

CIRCULAR

Date: 25/06/2015

The DUGC members are required to attend the meeting to be held on 11/06/2015 (Thursday) in the department to approve the syllabus of **IP Networking** for data/voice/video offered as core elective to the final year students of ECE Dept.

Following are the DUGC members

SL NO	NAME OF THE FACULTY	DESIGNATION
1.	Dr.S.Sandya	Chairperson
2.	Prof.Sitaram Yaji	Member
3.	Mr. Sankar Dasiga	Member
4.	Ms.Soumya .M	Member
5.	Ms.Shylaja	Member

Venue: R&D lab

Time: 3.00 P.M

HoD, ECE

(Dr.Sandya. S) 25/6/15

Head,
Department of Electronics & Communication Engg
Nitte Meenakshi Institute of Technology
Govindapura, Yelabanka
Bangalore - 560 064

ACADEMIC YEAR: 2015-2016(APRIL)

Sl No.	NAME	DESIGNATION	AFFLIATION	MEMBER
1	Dr Sandya S	Professor and Head, BOE Chairman	NMIT, Bangalore	Internal
2	Dr.Shankarananda			VTU Nominee
3	Dr Rathna	Principal Research Scientist	IISc, Bangalore	External
4	Dr N C Shivaprakash	Chief Research Scientist	IISc, Bangalore	External
5	Ms Divya J	Research Associate	Center for Small Satellite Research, NMIT, Bangalore	Alumni Nominee
6	Dr K N Haribhat	Professor	NMIT, Bangalore	Internal
7	Dr Prashanta H S	Professor	NMIT, Bangalore	Internal
8	Dr Sreenivasappa	Professor	NMIT, Bangalore	Internal
9	Prof. SankarDasiga	Professor	NMIT, Bangalore	Internal
10	Prof.MahaviraSwamy	Professor	NMIT, Bangalore	Internal
11	Prof.SitaramYaji	Professor	NMIT, Bangalore	Internal
12	Ms Veda	Assoc. Professor	NMIT, Bangalore	Internal
13	Ms Manjula	Assoc. Professor	NMIT, Bangalore	Internal
14	Ms Naina	Assoc. Professor	NMIT, Bangalore	Internal
15	Mr Shashidhar	Assoc. Professor	NMIT, Bangalore	Internal
16	Ms RekhaPadhke	Assistant Professor	NMIT, Bangalore	Internal

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560094

BoS Meeting

Date: 17/04/15

The BoS meeting for the academic year 2015 was held in the department of Electronics and Communication Engg on 17/04/15 for the approval of scheme and syllabus of III and IV semester.

Following external members were present

Dr.Rathna C.N, Principal Research Scientist,IISC Blore.

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- 1) Dr.Sandya S
- 2) Dr.Prasahantha H.S
- 3) Prof Sankar Dasiga
- 4) Dr.Sreenivasappa
- 5) Dr.HariBhat
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- 7) Ms.Veda
- 8) Ms.Manjula
- 9) Ms.Naina
- 10) Mr.Shashidhar
- 11) Ms.Rekha Phadke

The following points were discussed.

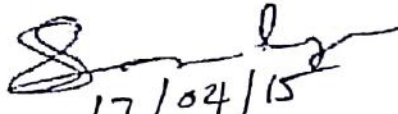
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Head,
Department of Electronics & Communication Engg.
K. J. Somaiya Institute of Technology
Gandhinagar, Velhanka
Bapatkhal - 400064

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10. Fields and Waves to be retained in IV semester
11. In Microcontroller -I , ensure that each unit content is adequate for 9 hrs. of distribution so that 20 marks question from each is feasible to be given
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15. MC LAB -1 , be specific about which experiment to be done in assembly language AND using C , also be specific which experiment are to be done using 8051 and which with MSP430

HoD,ECE


17/04/15

(Dr.Sandya S)

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 067

NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION
BOARD OF STUDIES Year-2016
PANEL MEMBERS

14/5/2015

Date of BoS meet	14 th MAY 2016
Members	
External	1. Dr. Rathna C.N Principal Research Scientist, IISC Blore 2. Dr. N.C ShivaPrakash, Chief Research Scientist, IISC. Blore 3. Mr. Purushothaman, KPII 4. Mr. Somashekar, Analog semiconductors
Internals	1) Dr. Sandya S 2) Dr. Prasantha H.S 3) Prof Sankar Dasiga 4) Dr. Sreenivasappa 5) Dr. Hari Bhat 6) Prof. Mahayira Swamy 7) Prof. Sitaram Yaji 8) Mr. Rajesh 9) Mr. Shashidhar

NMIT Alumni 2015 - Mackton Vishal

Time: 9.00 am

Venue: R & D lab

HOD ECE

(Dr. Sandya S)

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelankank
Bangalore - 560 064.




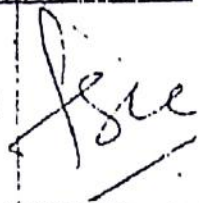
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NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

External BoS members

Date: 14/05/2016

Sl no	Name member	Organization	Area of interest	Email id	Signature
1	Dr.Rathna C.N	IISc	DSPProcessors, Embedded systems	rathna@ee.iisc.ernet.in	
2	Dr.N.C ShivaPrakash	IISc	Electronics, Analytical instrumentation	shiv@iap.iisc.ernet.in	
3	Mr.Purushothaman Surendran	KPIT	Embedded Systems	purushothman.surendran@kpit.com	
4	Somashckar B	Analog Semiconductor	Analog Design	soma@analog-semi.com	

Head,
Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064

Date: 27/08/2014

Department of Electronics and Communication Engineering

A DUGC meeting was held on 27/08/2014 for the approval of change in syllabus of the following subjects

- 1) Digital electronics- 3rd sem
- 2) DSD using Verilog-4th sem

Following members were present

DUGC MEMBERS

SL NO	NAME OF THE FACULTY	DESIGNATION
1.	Dr.S.Sandya	Chairperson
2.	Prof. N. Mahavira Swamy	Member
3.	Dr. Mrinal Sarvagya	Member
4.	Prof.Wilfred	Member
5.	Dr. Rukmini	Member
6.	Dr. Sreenivasappa	Member
7.	Mr. Sankar Dasiga	Member

Following points were discussed:

- 1) New topics such as memory and programmable logic devices introduced in **Digital Electronics** subject was approved by the committee as it is required for higher semester courses.
- 2) Topics related to **FPGA** introduced in the Vth unit of Digital system design using verilog was acceptable to the committee.

The revised syllabus of the above subjects is attached.

HOD, ECE

(Dr.Sandya.S)

Head,

Department of Electronics & Communication Engg.
Nitte Meenakshi Institute of Technology
Govindapura, Yetahanka
Bangalore - 560 064

NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY

Department of Electronics and Communication Engg

Date:25/06/2014

BoS COMMITTEE (2014-15)

External members

1. Dr. Anand Mohan
2. Dr. Vedavathy
3. Dr. Sadanand Gulwadi

Internal members

1. Dr. H.C. Nagaraj
2. Dr. Sandya S
3. Prof. N. Mahavira Swamy
4. Dr.Sreenivasappa
5. Dr. Mrinal Sarvagya
6. Dr.S.L Pinjare
7. Dr.Punitavathi
8. Dr.Rukmini T.S
9. Prof.G.H Sarma
10. Ms.Rekha Phadke


25/6/2014
HoD, ECE
Head,

Department of Electronics & Communication Engg
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064



Department of Electronics and Communication Engineering

27/6/2014

Minutes of Special BoS Meeting:

Date: 25/06/ 2014

Venue: R&D Lab of Dept of ECE

External Experts: Dr. Anand Mohan, Dr. Vedavathy, Dr. Sadanand Gulwadi

Members of Faculty of Dept of ECE

Points Noted:

- **Basic Electronics:**
 - The proposed updates from the department are i) rearrange the units / topics so as to cover the number system first, ii) drop the **OP-AMP** based differentiator and integrator, as these topics are considered not relevant for learning for students of non-ECE branches, iii) introduce basics of digital communication
 - Inputs from external experts: i) Introduce sequencers and counters in Unit 1, ii) Units 2 and 3 are too in-depth which may not be relevant to students of non-ECE branches, iii) Broad-base the syllabus so that non-electronics students could relate to the modern / current day electronics world by introducing topics such as CMOS, IC Technology, Wireless and Cellular technologies / terminology, iv) Do not add topics in this course so as to ease / help the labs of Physics course!! (Rather the syllabus of any course, Physics here, should be self-contained!!!)
 - Action Item(s): Syllabus topics to be updated accordingly and shared

1
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with the external experts

- **Digital Electronics:**

- Inputs from external experts: i) Introduce FPGA, ii) Correct many formatting, spelling and naming errors in the list. For, rename the topic 'Boolean Algebra Theorem' to more meaningful and understandable 'De Morgan theorem'
- Action Item(s): Updated list to be shared with the external experts

- **Analog Electronic Circuits:**

- Inputs from external experts: i) Introduce CMOS based OP-AMPS and OP-AMP comparator, ii) The in-depth topics taken out from the basic electronics course are to be added to the list of topics here!!, iii) The book: CMOS Analog Circuit Design by P.E. Allen and D.R. Holberg could be added as reference

- **Digital System Design with VERILOG**

- Inputs from external experts: i) in general a programming language specific course has to be avoided!! The choice of a particular programming language comes up upon a problem based assignment / hands-on is to be solved by the student which, he / she is expected to pick-up as a step of completing the exercise!!

- **Microprocessor**

- Inputs from external experts: i) An academic course cannot be based on the architecture / specifics of a processor such as 8086, ii) It should be considered to re-name / re-orient this course as "Computer Architecture" and cover such topics as pipelining, GPU architecture, memory organizations such as Harvard and Von Neumann. Use text book such as Huang A Briggs.
- Action Item(s): Proposed list for the suggested course to be prepared

and shared with the external experts

- **Antennas and Wave Propagation**

- The proposed updates from the department are i) Introduce adaptive and smart antennas
- Inputs from external experts: i) Introduce RF and CMOS

Common / Generic Inputs:

- Do not use any abbreviations in the list of topics that would confuse the students and any new faculty taking-up the subject.
- Ensure that each list of topics is formatted, free of spelling mistakes, and, more importantly appropriately ordered / sequenced!! For this, the list could be compiled by referring the list of contents from a standard text book!!!
- Any new topic introduced should be from / based on a standard text book
- Major changes / improvements suggested by the external experts could be incorporated progressively per the institutional guidelines, ramp-up by the department and teaching faculty
- Syllabus updates as suggested / discussed above are to be completed by respective members of faculty by 8/7/14

S. Srinivas
27/6/2014
HoD, ECE

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Bangalore - 560 064

Nitte Meenakshi Institute of technology

Yelahanka, Bangalore



Department of Electronics and Communication Engineering

Minutes of Special BoS Meeting:

Date: July 4th, 2014

Venue: R&D Lab of Dept of ECE

Present: External Experts: Dr. Anand Mohan, Dr. Ratna, Dr. Sadanand (ARM)

Members of Faculty of Dept of ECE

Points Noted:

Basic Electronics:

The proposed updates from the department are i) rearrange the units / topics so as to cover the number system first, ii) drop the OP-AMP based differentiator and integrator, as these topics are considered not relevant for learning for students of non-ECE branches, iii) introduce basics of digital communication

Inputs from external experts: i) Introduce sequencers and counters in Unit 1, ii) Units 2 and 3 are too in-depth which may not be relevant to students of non-ECE branches, iii) Broad-base the syllabus so that non-electronics students could relate to the modern / current day electronics world by introducing topics such as CMOS, IC Technology, Wireless and Cellular technologies / terminology, iv) Do not add topics in this course so as to ease / help the labs of Physics course!! (Rather the syllabus of any course, Physics here, should be self-contained!!!)

Action Item(s): Syllabus topics to be updated accordingly and shared with the external experts

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2014

Digital Electronics:

Inputs from external experts: i) Introduce FPGA, ii) Correct many formatting, spelling and naming errors in the list. For, rename the topic 'Boolean Algebra Theorem' to more meaningful and understandable 'De Morgan theorem'

Action Item(s): Updated list to be shared with the external experts

Analog Electronic Circuits:

Inputs from external experts: i) Introduce CMOS based OP-AMPs and OP-AMP comparator, ii) The in-depth topics taken out from the basic electronics course are to be added to the list of topics here!!, iii) The book: CMOS Analog Circuit Design by P.E. Allen and D.R. Holberg could be added as reference

Digital System Design with VERILOG

Inputs from external experts: i) in general a programming language specific course has to be avoided!! The choice of a particular programming language comes up upon a problem based assignment / hands-on is to be solved by the student which, he / she is expected to pick-up as a step of completing the exercise!!

Microprocessor

Inputs from external experts: i) An academic course cannot be based on the architecture / specifics of a processor such as 8086, ii) It should be considered to re-name / re-orient this course as "Computer Architecture" and cover such topics as pipelining, GPU architecture, memory organizations such as Harvard and Von Neumann. Use text book such as Huang A Briggs.

Action Item(s): Proposed list for the suggested course to be prepared and shared with the external experts

Antennas and Wave Propagation

The proposed updates from the department are i) Introduce adaptive and smart antennas

Inputs from external experts: i) Introduce RF and CMOS

Linear Integrated Circuits

Following topics need to be added V to I and I to V converters, Precision rectifiers, Clamping circuits, peak detectors, Sample and hold circuit, Differentiator, integrator.

Radar Engineering

A course on Radar engineering was introduced for 6 sem as core elective. The syllabus includes basics of Radar and also different parameter used in Radar engineering.

Cryptography

A course on Cryptography introduced for 8 sem students as core elective.

ARM Cortex

A course on ARM Cortex introduced for 7 sem as core elective. The objective of the course is to teach students how an ARM processor and its programming techniques are useful in the embedded applications in industry.

Common / Generic Inputs:

- Do not use any abbreviations in the list of topics that would confuse the students and any new faculty taking-up the subject.
- Ensure that each list of topics is formatted, free of spelling mistakes, and, more importantly appropriately ordered / sequenced!! For this, the list could be compiled by referring the list of contents from a standard text book!!!
- Any new topic introduced should be from / based on a standard text book
- Major changes / improvements suggested by the external experts could be incorporated progressively per the institutional guidelines, ramp-up by the department and teaching faculty
- Syllabus updates as suggested / discussed above are to be completed by respective members of faculty by 8/7/14

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Bangalore - 560 064

Department of Electronics and Communication Engineering

CIRCULAR

Date: 5/05/12

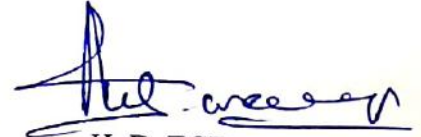
The internal BoS members are required to attend the meeting to be held on 07/05/12 to incorporate the changes suggested in BoS 2012-13

Following are the BOS members

BoS MEMBERS		
SL NO	NAME OF THE FACULTY	DESIGNATION
1	Prof.MahaviraSwamy	Chairman
2	Dr.Sreenivasappa	Member
3	Dr.S.L pinjare	Member
4	Ms.Veda	Member
5	Mr.Rajesh	Member
6	Ms.Soumya M	

Venue: R&D lab

Time: 3.00 P.M


HoD, ECE

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Govindapura, Yelahanka
Bangalore - 560 064

Date: 07/05/2012

Department of Electronics and Communication Engineering

A internal BoS meeting was held on 07/05/2012 to incorporate the changes suggested in BoS 2012-13

Following members were present

BoS MEMBERS		
SL NO	NAME OF THE FACULTY	DESIGNATION
1	Prof.MahaviraSwamy	Chairman
2	Dr.Sreenivasappa	Member
3	Dr.S.L pinjare	Member
4	Ms.Veda	Member
5	Mr.Rajesh	Member
6	Ms.Soumya M	

Following are the changes incorporated as per the discussion in BOS 2012-13

1. The Syllabus of **MEMS** was presented by Dr.S.L Pinjare , Ms.Soumya M. It was offered as elective for 5 sem students
2. The syllabus of **MSP 430** was framed and presented by Dr.Sreenivasappa. It was offered as elective for 8 sem students.



HoD,ECE

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BOARD OF STUDIES

MINUTES OF MEETING TO DESIGN THE CURICULLUM FOR V-VIII SEMESTER

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

The Board of Studies meeting was conducted on 5/5/2012 at 10:30 a.m. in R&D Lab of the Department of Electronics and Communication Engineering. The following External Member of the BOS attended the meeting

1. Dr. Anand Mohan
2. Dr. Vedavathy
3. Dr. Puttamadappa
4. Dr. Sadanand Gulwadi
5. Mr. Shri Hari Bhat

The meeting was also attended by the following internal members

1. Dr. H.C. Nagaraj
2. Prof. N. Mahavira Swamy
3. Dr. Chirag Sharma
4. Dr. Mrinal Sarvagya
5. Prof. G.H. Sarma
6. Prof. Sankar Dasiga
7. Prof. Sreenivasappa B.V.
8. Prof. Veda Sandeep Nagaraja

After going through the syllabus following suggestions/Comments were made

General Comments on 3rd and 4th Semester Subjects

Since the BOS was not in a position to make corrections and amendments for 3rd and 4th Semester subjects, the committee members gave only the following general suggestions.

- Have computer organization as 3rd semester core subject & book authored by Patterson is recommended
- Include microprocessor / microcontroller in 4th semester.
- In microcontroller include 2 units of MSP 430.
- The embedded system course flow in the curriculum should have the following hierarchy
 - First a general processor architecture
 - RTOS
 - SOC
 - VLSI design using any CAD tool

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Include MATLAB simulation experiments as assignment for the following subjects :

- **Control Systems**
- **Network Analysis**
- **Field theory**
- **Signal and Systems**
- **DSP**
- **Analog Communication**
- **Linear Integrated Circuits**
- **Microwave and Radar (Smith chart)**
- **Digital Communication**
- **Wireless Communication**
- **Antenna and Wave Propagation**
- **Power Electronics**
- **Information Theory and Coding**

5th Semester

Control Systems

- **Include latest edition of text books in the syllabus**
- **Remove books authored by Mr.Bakshi as reference book.**

Analog Communication

- **Random Process chapter in the first unit to be removed completely or modified and reduced.**

Microwave Engineering and Radar

- **Correct the name of the subject in the scheme. It should be written as Microwave Engineering and Radar**
- **Syllabus is huge in the subject, needs to be reduced.**
- **More emphasis should be given to unit IV**
- **Less emphasis on unit II**
- **Relook into devices chapter. Lay emphasis only on Gun Diode and micro strip and remove other devices that are not used any more in industry. Include TWT, Reflex Klystron & Magnetrons. Also include GaAs FET's.**
- **Remove 3rd text book**
- **Include K.C. Gupta text book.**

Fundamentals of VLSI Design

- **Unit I- should be on MOS theory**
- **Include standard cell design concept in unit I**
- **Include digital part like clocking, asynchronous interface etc.**

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- Unit III – include datapath elements and remove redundant parts.
- Include design concepts otherwise remove design from the title
- Assignment should be given on spice simulations and layout and that to be included in the syllabus.

Data Structures Using C

- All the committee members agreed that this subject needs to be included as a core subject for the Vth semester students.
- Correct the title of the course. It is C and not C++

General comments for 5th Semester subjects

- Include all the latest edition books as reference and text book.
- Relook into the syllabus of embedded systems

6th Semester

Computer Communication Network

- Unit I to be modified. Important topics of Digital Switching system to be included.
- Tannenbaum should be included as reference
- Include latest edition of Forouzan.
- Include Bluetooth and Zigbee by replacing some of the Ethernet protocols.
- Unit V to be modified.
- Include MPLS.
- Layer 2 modern protocols, VOIP to be included.
- Include Quality of Service
- Include Network Security concepts.

Digital Communication

- Include Prokias as text book.
- Try to modify DC syllabus since it is vast.
- Include latest edition as the text book and reference books.
- Include book authored by Mr.Radha Krishna Rao as reference as it has MATLAB examples.

Antenna and Wave Propagation

- Give less emphasis on point sources and more emphasis on array sources.
- More emphasis should be given on microstrip antenna, electric dipoles and arrays.
- Assignment can be given using MATLAB and HFSS tool.
- No analysis required on helical antenna. Give only concept and principle. Same is true for Yagi Uda and some other basic antenna. Log Periodic antenna may be mentioned.
- Lay more emphasis on antenna that are currently widely used. Give analysis only for those antenna.
- Relook unitIV with above amendments.
- Include Antenna measurements in unit IV.

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- Propagation chapter should be taught from text book authored by Jordhan
- Communication using Troposphere can be removed from unit V & ionosphere propagation to be discussed in detail.
- Balani text book is difficult to interpret, so remove it from text book and include as reference.
- Include latest edition of all text and reference books.
- Dr. Vedavathy has offered to give material for the subject.

7th Semester

Fiber Optic Communication

- Include Optical networks in one unit.
- Dr. Anand Mohan and Dr. Mrinal to give contact for Tejas Network.
- Include some concepts of telecom network.
- Include latest concepts in one unit.
- Redo the entire syllabus.

Information Theory and Coding

- LDPC to be included.
- Include architectures encoding schemes.
- Castilo book has to be included.
- Assignment to be given using MATLAB, C and C++.

Power Electronics

- In introduction once power devices is mentioned, it should include all devices including power BJT. So there is no need for separate chapter on that.
- Include triggering circuits such that it supplements the lab experiments.
- If the theory syllabus does not cover parallel and series inverter syllabus then remove it from the lab.
- SMPS to be included in the syllabus.
- Include battery management
- Include 2010 edition of Rashid text book.

8th Semester

Wireless Communication

- Unit IV to be removed as it is taught in digital communication.
- Include diversity and equalization techniques.
- Redo Unit V: details of CDMA, MIMO, OFDM to be included in unit V.
- In unit IV GSM & CDMA should be covered in detail.
- Factors for designing base station antenna to be included.
- Evolution of wireless technology to be included in unit I.
- Include system based technology in unit I.

Electives

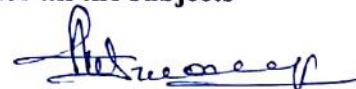
- Electives offered should be based on the streams chosen by the student.

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- Have no duplication of syllabus in core and electives.
- Computer organization subject include ARM concepts.
- Instrumentation syllabus include Biomedical applications.

General Comments

- It was observed that weightage given to practical is very less.
- Hence the members advised to combine surprise test marks and assignment marks i.e. give 20 marks for experiment based assignment.
- There should be emphasis for soft skill training.
- Value added courses should be included in lower semesters.
- Include latest edition of text books and reference books for all the subjects



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Yelahanka, Bangalore



Department of Electronics and Communication Engineering

Minutes of Special BOS Meeting to design the curriculum for V-VIII semester

Date: May 3rd, 2012

Venue: R&D Lab of Dept of ECE

Members Present: **Dr. C P Ravikumar, Director, UNITI**

All Faculty of Dept of ECE

Points Discussed:

1. Content / syllabus of the Course: **FUNDAMENTALS OF VLSI DESIGN** (10EC54) could further be strengthened by including Unit I of the Elective Course: ASIC Design (10ECE824)
2. The courses on **Microprocessors and Microcontrollers** could be combined and offered as “Microcontrollers and Microprocessors I” and “Microcontrollers and Microprocessors II” can be taught in III & IVth semester respectively. The courses could include MSP430, ARM, Atom etc. However for the present batch of students the above subjects viz **MSP430, ARM** are taught in V & VIII semesters respectively
3. Inclusion of the course on **Data Structures** is necessary as otherwise students of ECE will be at disadvantageous position compared to students of CSE, hence it is introduced as core subject for Vth semester students.
4. It is important to have power electronics and control systems as the core courses for the ECE branch.
5. **Transducers and Instrumentation** is also an important course but, unfortunately the department is not in a position to have it as a core subject, but introduced as Elective for Vth semester. In addition department was advised to consider introducing other topics of relevance as one unit of value-added courses, and have the classes during the weekends / holidays during the semesters.
6. When new courses are being introduced the faculty members who would be handling them could consider arranging curriculum development workshops (It is the recommended way of doing).
7. The department could consider inviting experts from industry for delivering talks on the emerging technological trends and consider awarding credits to students who attend these lectures and submit a report on the learnings.

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Bangalore - 560 064

8. Members of the faculty may look at cnx.org of Rice University for manuals / procedures on various experiments that could be introduced ,to setup in various lab courses.

Additional Inputs:

- ❖ Popular and widely referred book: ASIC by M J S Smith, is now available on the web, downloadable free of cost.
- ❖ cc430 , cc2000, cc3000, cc4000 boards of TI could be considered for introducing experiments on Zigbee, BT, WiFi and GPS in the Advanced Communications lab of 6th semester. Dr. K Radhakrishna Rao who is currently with TI, Bangalore could be contacted for any further inputs needed on these boards
- ❖ TI along with CDAC, Hyderabad is organizing a faculty development program on ARM at Hyderabad during June 2012
- ❖ On June 6th, 2012 TI is organizing a faculty development program on Beagle board at Bangalore
- ❖ For introducing the 1 unit courses, the models used by BMS College of Engineering and PSG College of Tech could be looked at.


HOD, ECE

Kind Attn: Principal

Head,
Department of Electronics & Communication Engg.
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Bangalore - 560 064

Kind Attn: Director

**NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

Program: M.Tech (VLSI Design and Embedded Systems)

New courses introduced in M.Tech VLSI Design and Embedded Systems during the last five years

Name of the Course	Name of the Programme	Weather this course is a new course introduced during the last five years (Yes/No)	Year of Introduction
SEMINAR	M Tech VLSI Design and Embedded Systems	YES	2016-17
SEMINAR/FIELD WORK/PROFESSIONAL TRAINING/ SELF STUDY/TERM PAPER	M Tech VLSI Design and Embedded Systems	Yes	2016-17
PROJECT PHASE -1	M Tech VLSI Design and Embedded Systems	Yes	2016-17
PROJECT PHASE -2- THESIS ASSESMENT	M Tech VLSI Design and Embedded Systems	YES	2016-17
PROJECT PHASE -2- INTERNAL EVALUATION AND VIVO VOCE	M Tech VLSI Design and Embedded Systems	Yes	2016-17
VLSI Process Technology	M Tech VLSI Design and Embedded Systems	YES	2014-15
Automotive Electronics	M Tech VLSI Design and Embedded Systems	YES	2014-15
Image & Video Processing	M Tech VLSI Design and Embedded Systems	Yes	2014-15
ARM Architecture and Programming	M Tech VLSI Design and Embedded Systems	YES	2018-19
Algorithms for VLSI Design	M Tech VLSI Design and Embedded Systems	YES	2018-19
Advanced Embedded Systems Lab	M Tech VLSI Design and Embedded Systems	YES	2014-15
Embedded System Microcontroller - Architecture and Software	M Tech VLSI Design and Embedded Systems	YES	2018-19
VLSI Physical Design	M Tech VLSI Design and Embedded Systems	YES	2016-17
Machine Learning for Pattern Recognition	M Tech VLSI Design and Embedded Systems	yes	2018-19
VLSI for Signal Processing	M Tech VLSI Design and Embedded Systems	YES	2018-19
Research Methodology and IPR	M Tech VLSI Design and Embedded Systems	YES	2014-15

Department of ECE, NMIT/New Courses Offered

Self-Study MOOC	M Tech VLSI Design and Embedded Systems	YES	2016-17
Advance Mathematics	M Tech VLSI Design and Embedded Systems	YES	2014-15
CMOS VLSI Design	M Tech VLSI Design and Embedded Systems	YES	2014-15
Advanced Embedded System	M Tech VLSI Design and Embedded Systems	YES	2014-15
Digital System Design using Verilog	M Tech VLSI Design and Embedded Systems	YES	2014-15
MEMS and NanoElectronics	M Tech VLSI Design and Embedded Systems	YES	2014-15
Term Project	M Tech VLSI Design and Embedded Systems	YES	2016-17
Design of Analog and Mixed Mode VLSI Design	M Tech VLSI Design and Embedded Systems	YES	2014-15
Advance MicroController	M Tech VLSI Design and Embedded Systems	YES	2016-17
LINUX for Embedded systems	M Tech VLSI Design and Embedded Systems	YES	2016-17
Low Power VLSI Design	M Tech VLSI Design and Embedded Systems	YES	2014-15
VLSI Design and Embedded System Lab - 2	M Tech VLSI Design and Embedded Systems	YES	2014-15

Signature and Seal
HoD, ECE

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Bangalore - 560 064

Program: M.Tech (Digital Communication and Networking)

New courses introduced in M.Tech Digital Communication and Networking during the last five years

Name of the Course	Name of the Programme	Weather this course is a new course introduced during the last five years (Yes/No)	Year of Introduction
Advanced Mathematics	M Tech Digital Communication and Networking	YES	2016-17
Advanced Digital Communication	M Tech Digital Communication and Networking	Yes	2016-17
Advanced Embedded System	M Tech Digital Communication and Networking	YES	2016-17
Antenna Theory & Design	M Tech Digital Communication and Networking	YES	2016-17
Applied information theory & coding	M Tech Digital Communication and Networking	YES	2016-17
Wireless Communication	M Tech Digital Communication and Networking	Yes	2016-17
RF & Microwave Circuit Design	M Tech Digital Communication and Networking	YES	2016-17
Artificial Neural networks	M Tech Digital Communication and Networking	YES	2016-17
Advanced computer networks	M Tech Digital Communication and Networking	YES	2016-17
SEMINAR/FIELD WORK/PROFESSIONAL TRAINING/SELF STUDY/TERM PAPER	M Tech Digital Communication and Networking	YES	2016-17
PROJECT PHASE -1	M Tech Digital Communication and Networking	Yes	2016-17
PROJECT PHASE -2- THESIS ASSESMENT	M Tech Digital Communication and Networking	YES	2016-17
PROJECT PHASE -2- INTERNAL EVALUATION AND VIVO VOCE	M Tech Digital Communication and Networking	YES	2016-17
Advanced Info Theory & Coding	M Tech Digital Communication and Networking	YES	2018-19
Automotive Electronics	M Tech Digital Communication and Networking	YES	2018-19
Image & Video Processing	M Tech Digital Communication and Networking	YES	2018-19
Network Security	M Tech Digital Communication and Networking	YES	2018-19

Internet of Things	M Tech Digital Communication and Networking	YES	2018-19
Software Defined Radio	M Tech Digital Communication and Networking	YES	2018-19
Spread Spectrum Communication	M Tech Digital Communication and Networking	YES	2018-19
Machine Learning for pattern reorganization	M Tech Digital Communication and Networking	YES	2018-19
Advanced Digital Signal Processing	M Tech Digital Communication and Networking	YES	2018-19
Communication Design Lab	M Tech Digital Communication and Networking	YES	2018-19
Research Methodology and IPR	M Tech Digital Communication and Networking	YES	2018-19
Self-Study MOOC	M Tech Digital Communication and Networking	YES	2018-19
Antenna Theory and Design	M Tech Digital Communication and Networking	YES	2016-17
Applied Information Theory and Coding	M Tech Digital Communication and Networking	YES	2016-17
Satellite communication	M Tech Digital Communication and Networking	YES	2016-17
OPTICAL FIBER COMMUNICATION	M Tech Digital Communication and Networking	YES	2016-17
Advanced Signal Processing	M Tech Digital Communication and Networking	YES	2016-17
Error control coding	M Tech Digital Communication and Networking	YES	2016-17
MULTIMEDIA COMMUNICATION	M Tech Digital Communication and Networking	YES	2016-17
Network Programming	M Tech Digital Communication and Networking	YES	2016-17
Multimedia networks	M Tech Digital Communication and Networking	YES	2016-17
Spread spectrum communication	M Tech Digital Communication and Networking	YES	2016-17
Cryptography and network security	M Tech Digital Communication and Networking	YES	2016-17
Seminar/Field work/Professional training/Self Study/Term Paper	M Tech Digital Communication and Networking	YES	2016-17
Project Phase-1	M Tech Digital Communication and Networking	YES	2016-17
Project Phase-2/Thesis Assessment	M Tech Digital Communication and Networking	YES	2016-17
Project Phase 2 -Internal Evaluation and Viva Voce	M Tech Digital Communication and Networking	YES	2016-17

Antenna Theory and Design	M Tech Digital Communication and Networking	YES	2014-15
Probability and Random Process	M Tech Digital Communication and Networking	YES	2014-15
Advanced Digital Communication	M Tech Digital Communication and Networking	YES	2014-15
Wireless and Mobile Networks	M Tech Digital Communication and Networking	YES	2014-15
Automotive electronics	M Tech Digital Communication and Networking	YES	2016-17
DEC Lab -1	M Tech Digital Communication and Networking	YES	2014-15
Seminar on Advanced topics from refereed journals	M Tech Digital Communication and Networking	YES	2014-15
Wireless Communication	M Tech Digital Communication and Networking	YES	2014-15
RF and Microwave circuit design	M Tech Digital Communication and Networking	YES	2014-15
Modern DSP	M Tech Digital Communication and Networking	YES	2014-15
Optical Communication and Networking	M Tech Digital Communication and Networking	YES	2014-15
DEC Lab -2	M Tech Digital Communication and Networking	YES	2014-15
Seminar on Advanced topics from refereed journals	M Tech Digital Communication and Networking	YES	2016-17
Midterm Presentation on Internship	M Tech Digital Communication and Networking	YES	2016-17
Report on Internship	M Tech Digital Communication and Networking	YES	2016-17
Evaluation and Viva-Voce	M Tech Digital Communication and Networking	YES	2014-15
Error control coding	M Tech Digital Communication and Networking	YES	2014-15
Evaluation of Project Phase-1	M Tech Digital Communication and Networking	YES	2014-15
Phase-II : Midterm evaluation of Project	M Tech Digital Communication and Networking	YES	2014-15
Evaluation of project work and Viva - Voce	M Tech Digital Communication and Networking	YES	2014-15



Signature and Seal

HoD, ECE
Head,

Department of Electronics & Communication Engg
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
Bangalore - 560 064



TITLE: Minutes of Meeting	DESCRIPTION: PG Internal BOS Meeting	Year: 2018	Date: 19/11/18	Pa 1/
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- M.Tech II Syllabus and scheme to be updated considering the industry requirements.
- Training in Matlab, C programming, Embedded system, Hardware and software co-design, FPGA is required for KPIT.
- Previous batch 50% of students did their internship at IISC.
- Current batch 50% of students are doing their internship at KPIT.
- From placement point of view mobile communication to be included for DCN.
- Industry oriented courses to be included to increase the placement.
- Machine learning course contents to be finalised by Dr.Jayavrinda and Dr.Raghunandan.
- Draft syllabus content to be ready for IOT and ML.
- Suggested to include DRDO members for DCN BOS panel.
- A few good mathematics contents to be revisited from placement point of view. Matlab assignment to be given.(30+20)
- Seminar on Modilica tool to be scheduled by Mr.Shashidhar.
- Automotive electronics is common for both DCN and VLSI program. Tool based assignment to be given.
- DSD using Verilog tool based assignment to be given.
- Faculty should share the tool based assignment and details of software required.
- Assignment based labs to be conducted and attendance during assignment labs to marked under special attendance in Gurukul.
- FPGA based system design syllabus to be framed considering industry requirements and VTU syllabus for both PG and UG.

Rine

S. W. (for HoD)
HoD, Dept. of ECE

BOARD OF STUDIES

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

2017-18

Date:12/05/17

Date of BoS meeting	9 th MAY 2017	Expertise
MEMBERS		
External	1) Dr.Rathna G.N,IISC	Communication and signal Processing
	2) Dr.Ravish Aradhya, Prof,RVCE	VLSI Design and Embedded systems
Student alumni	1) Ms.Pruthvi, OSI energy Automation LTD	Embedded systems
	2) Mr.Anandtheerth. S. Mathad, NMII	Communication
Chairman	Dr. Sandya S, HoD, Dept ECE	Communication and Embedded Systems
internal	1) Dr. S.L Pinjare	VLSI

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	2) Dr.Raghunandan	Communication
	3) Prof. Sankar Dasiga	Embedded Systems
	4) Dr.Rukmini	Communication
	5) Dr.Veda Nagraj	VLSI, MEMS
	6) Prof. MahaviraSwamy N	Communication

Dr.Sandya S welcomed all the BoS members.

Agenda of the Board of Studies meeting 2017-18

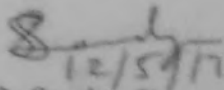
1. Approval of scheme and syllabus for UG VII-VIII sem 2014-18 batch
2. Approval of syllabus of Basic Electronics for the 2017-2021 batch
3. Approval of scheme and syllabus for PG programs
 - i) VLSI Design and Embedded system
 - ii) Digital Communication and Networking

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Minutes of BoS meeting –PG VLSI Design and Embedded Systems

1. Dr Ravish Aradhya and Dr Rathna suggested that students term project shall be rolled out as a paper
Action: Inputs shall be considered
2. The Advanced Mathematics subject content is to be revisited for VLSI stream.
Action: Shall be discussed in DPGC
3. Dr Ravish Aradhya suggested that a subject on Static Timing Analysis is to be introduced in 1st Sem.
Action: Inputs shall be considered and implemented for 2018-2020 batch
4. Dr Ravish Aradhya suggested introducing new elective subjects such as SOC, Embedded Networking and VLSI Testing & Verification for 3rd Sem.
Action: Inputs shall be considered and discussed in DPGC
5. For Low Power VLSI Design it was suggested to retain Adiabatic Circuits in the Syllabus.
Action: Inputs are considered and under execution

HoD, ECE


12/5/17
(Dr.Sandya S)

Head,
Department of Electronics & Communication Engr
Nitte Meenakshi Institute of Technology
Govindapura, Yelahanka
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Minutes of BoS meeting –PG Digital Communication and Networking

1. Dr Ravish Aradhya H.V and Dr Rathna raised concerns that there was no core subject on networking being offered in 1st Sem of DCN. It was suggested to move Advanced Embedded System to Elective group and offer Advanced Computer Networks as a core subject.

Action: Inputs Shall be considered and will be implemented for 2018-2020 batch

2. Members of the BOS suggested that RF and Microwave which is currently in 2nd Sem can be moved to 1st Sem and Antenna Theory and Design to 2nd Sem.

Action: Inputs Shall be considered and will be implemented for 2018-2020 batch

3. Anandtheerth –Alumini- PG, DCN suggested to introduce a subject on Simulation, Modelling and Analysis as an elective.

Action: Inputs shall be considered and will be discussed in DPGC

4. Members of the BOS were of the opinion that, the electives is to be re-arranged under two separate groups, namely Communication and Networking.

Action: Corrections shall be made

5. Dr Rathna suggested to introduce new subjects such as Wireless Sensor Network, SDN, SDR in 3rd Sem as Self Study Component, where during the first two weeks the faculty can give an introduction to the subject and in the remaining weeks on every Saturday the students can present papers from leading publishers on that subject.

Action: Inputs shall be considered and discussed in DPGC

6. Members of the BOS suggested that, Unit 4 and 5 of Advanced Mathematics is to be changed, and application specific topics such as Random Process, Probability etc. is to be included.

Action: Input Shall be considered and discussed in DPGC

7. Dr Ravish and Dr Rathna suggested that students term project shall be rolled out as a papers

Action:Inputs shall be considered

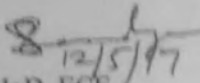
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Bangalore - 560 004

8. Dr Rathna suggested including topics on CNN in Artificial Neural Networks syllabus. And Artificial Neural Networks can be made common subject for both VLSI and DCN stream.

Action: Inputs Shall be considered and discussed in DPGC

9. For RF and Microwave subject, it was suggested to reorganize the contents, include double stub application, avoid overlapping with UG 5th Sem Microwave syllabus and to include Text 2 in reference and not as Text Book.

Action: Inputs are considered and corrections are made


12/5/17
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(Dr. Sandya S)

Head,
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

PG **List of External BoS members**

Date: 1/10/2016

Sl no	Name member	Organization	Area of interest	Email id	Signature
1.	Dr.Rathna C.N	IISC	DSP Processors, Embedded systems	rathna@ee.iisc.ernet.in	
2.	Dr.N.C ShivaPrakash	IISC	Electronics, Analytical instrumentation	shiv@iap.iisc.ernet.in	
3.	Dr.Bharadwaj Amrutur	IISC	Micro-Nano Electronics	amrutur@ece.iisc.ernet.in	
4.	Dr. Prabhakar T V	IISC	Communication Networks.	tvprabs@cedt.iisc.ernet.in	
5.	Mr.Somashekar B	Analog Semiconductors	Analog Design	soma@analog-semi.com	
6.	Dr.Purushothaman Surendran	KPIT	Embedded Systems	purushothman.surendran@kpit.com	
7.	Dr.Manjuntha Hebbar	BUOYANCI	Embedded Systems, VLSI and Communication	mhebbar@buoyanci.com	

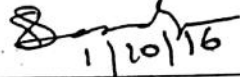

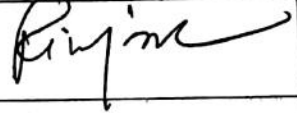
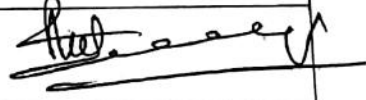
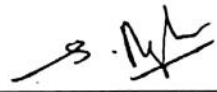
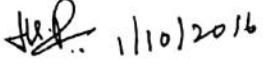
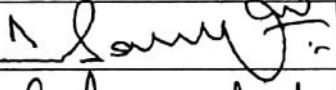
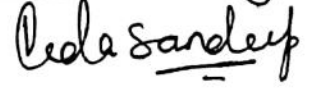
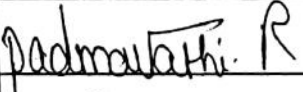

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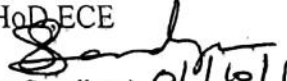
 (Dr.Sandhya) 01/10/16

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

List of Internal BoS members

Date: 1/10/2016




Sl.No	Name of the faculty	Designation	Signature
1.	Dr.Sandya S	Chairman BoS, Head of the ECE Department.	 1/10/16
2.	Dr.HariBhat	Professor , Dept of ECE	
3.	Dr.Rukmini	Professor , Dept of ECE	_____
4.	Dr.S.L.Pinjare	Professor , Dept of ECE	
5.	Prof.Sharma	Professor , Dept of ECE	_____
6.	Prof.Mahaveer Swamy	Professor , Dept of ECE	
7.	Dr.Raghunandhan	Professor , Dept of ECE	
8.	Dr.Prasahantha H.S	Professor , Dept of ECE	 1/10/2016
9.	Prof. Sankar Dasiga	Professor , Dept of ECE	
10.	Ms. Veda Sandeep Nagaraj	Assoc Prof , Dept of ECE	
11.	Dr.Padmavathi	Assoc Prof , Dept of Maths	
12.	Mr. Prasanna paga	Assoc Prof , Dept of ECE	

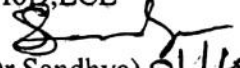
HoD ECE

(Dr.Sandhya) 01/10/16

NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

List of Students Alumini

Date: 1/10/2016

Sl.No	Name of the Student	Branch(stream)	Signature
1.	Mr.Kannan T	ECE, VLSI Design and Embedded systems	
2.	Mr. Arunkumar	ECE, VLSI Design and Embedded systems	
3.	Ms.Rashmi kulkarni	ECE, Digital Communication and Networking	

HoD,ECE

(Dr.Sandhya) 01/10/16


Dr Bharadwaj	- SW skills are critical; Basic C and Data structures are important
Dr Purushotthaman	- Project plays an important role - Critical mass needed – can't do much for a small strength
Dr Bharadwaj, Dr Shiva Prakash	- Reduce lecture hours, introduce more labs / tutorials - Should not have electives in first semester
Dr Rathna	- Should not have pre-requisites for any course in first semester
Dr Purushotthaman	- More MNCs want ES than VLSI
Dr Shiva Prakash	- What are the basic foundation courses (needed for both ES and VLSI, and which you should offer in first semester)?
Dr Purushotthaman	- More ES companies; so teach ES more in foundation / first semester
Dr Bharadwaj	- Yes, ES is needed for even Satellite research and Robotics research
Dr Somasekhar	- Where is uniqueness? Result: VLSI has severe shortage
Dr Shiva Prakash	- Can we change titles of courses? o Response from Prof Veda: No.
Dr Prabhakar	- Students should take online courses and these can be augmented by offline classes by teachers, who have taken up those courses themselves
Dr Bharadwaj, Dr Prabhakar	- Enable industry people to come and teach full courses / semesters
Dr Sandya	- Like IEEE e-blended programs
Dr Bharadwaj	- ES: Need FPGA to be taught. SCL gives facilities free for Academic institutions
Dr Somasekhar	- Semesters 1,2 & 3,4 have some imbalance, in terms of contact-hours versus credits - Suggestion: change number of credits in semesters as 26,26,24,24
Dr Rathna	- Rename mini-project as term-project - Foundation courses should not have pre-requisites; if you need students to know something, tell them and they should study, but don't write explicitly
Dr Bharadwaj Dr Shiva Prakash	- Maths syllabus – it is UG level, why repeat? What you need are things like Signals and Systems, Transforms, etc. - Need topics like scripting, automation, etc. as foundation courses
Dr Somasekhar	- Include things like Perl, Tcl/tk in foundation courses
Dr Shiva Prakash	- Math course to be revamped - Cover basics in Unit 1 in every course
Dr Purushotthaman	- ES: Real-time systems, RTOS, basic Embedded programming / Embedded Linux – needed to be taught for foundations in ES
Dr Somasekhar	- Can you separate VLSI and ES as two different M.Tech programs? - Change title of AES course
Dr Purushotthaman	- Suggestion for ES o Sem 1: Intro to ES, Emb Linux, etc o Sem 2: VxWorks, etc.
Dr Prabhakar	- Include in ES: Microcontrollers, Sensors, Actuators, Power supply, need Embedded System Design, I ² C, separate HW and SW courses, .. - Ref CMOS VLSI Design course – talk about non-VLSI also in Unit 1
Dr Somasekhar	- Teach few things but teach very well
Dr Bharadwaj	- Class hours should be for fundamentals
DCN Scheme and Syllabus review	
Dr Shiva Prakash	- Don't use "Advanced" as prefix in course titles
Dr Rathna Dr Prabhakar	- Tune Maths for each stream
Dr Shiva Prakash	- Networking is needed as "core", not only as elective

Dr Purushotthaman	- Change from Adv Computer NW to Adv Communication NW
Dr Prabhakar	- Teach NM1, NM2, MAC, ARQ, etc..... layer-wise ... Stop/Wait, Deep Learning, etc
Dr Shiva Prakash	- Teach machine learning
Dr Shiva Prakash Dr Purushotthaman	- Can you change from "VLSI & ES" and "DCN" to "VLSI" and "ES & DCN"? - Phase out some courses and Phase in some other courses
Dr Shiva Prakash	- You can have Signal processing as elective and NW Programming as core
Dr Purushotthaman	- We at KPIT re-teach same things after your students join us - Teaching needs to be strong - Try online courses – blend
Dr Bharadwaj	- Try open-book exams for better results
Dr Hebbar	- You have your research programs which are long-lasting. Based on those, you can design courses which will feed into / consistent with them.

Post the BoS meeting, there was a discussion between the HoD and the Director and Principal. It was decided to consider balancing the proportions of VLSI and ES components in the corresponding program.

Action items

#	Action item	Status / Remarks
1	VLSI versus ES – what is our emphasis? What do we want to be? 50-50? Different? Review course structure from the point-of-view of this decision.	
2	Identify "Foundation courses" – common for VLSI & ES	
3	Can we re-structure to offer all Foundation courses in First semester?	
4	Change titles (Example: to remove pre-fix "Advanced")	
5	Math course (now at UG level) to be revamped – and customize to streams. If this is not done, Math to be removed as mandatory course ..?	
6	Consider reducing lecture hours and increasing lab hours or introducing tutorial sessions	
7	Pre-requisites not to be mentioned in first semester. They need to be covered by students studying themselves or in first Unit by teacher	



 4/10/16
 Chairperson of BoS, ECE, NMIT
 and Head of Department, ECE, NMIT