NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

SCHEME FOR III-VIIIth SEMESTER (2014-2018)

SYLLABUS FOR III-IV th SEM(2014)

SEMESTER: III

Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1	14MAT31	ENGINEERING MATHEMATICS - III	BS	MAT	4	1	-	50	50	100	4
2	14 EC 32	ANALOG ELECTRONICS CIRCUIT	EC		4			50	50	100	4
3	14 EC 33	DIGITAL ELECTRONICS	PC		4			50	50	100	4
4	14 EC 34	NETWORK ANALYSIS	PC		4	1		50	50	100	4
5	14 EC 35	SIGNALS AND SYSTEMS	PC		4	1		50	50	100	4
6	14 EC 36	MICROPROCESSOR AND MICROCONTROLLER	PC		4			50	50	100	3
7	14ECL37	ANALOG ELECTRONICS LAB	PL		-	-	3	50	50	100	1.5
8	14 EC 38	DIGITAL ELECTRONICS LAB	PL		-	-	3	50	50	100	1.5
							TOTAL	400	400	800	26

SEMESTER: IV

Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1	14 EC 41	ENGINEERING MATHEMATICS - III	BS	MAT	4	1	-	50	50	100	4
2	14 EC 42	LINEAR INTERGRATED CIRCUIT	PC		4			50	50	100	4
3	14 EC 43	CONTROL SYSTEM	PC		4	1		50	50	100	4
4	14 EC 44	FIELD AND WAVES	PC		4	1		50	50	100	4
5	14 EC 45	DSD using VERILOG	PC		4			50	50	100	4
6	14 EC 46	MICROCONTROLLER	PC		4			50	50	100	3
7	14 EC L47	Microcontroller LAB	PL		-	-	3	50	50	100	1.5
8	14 EC L48	DSD using Verilog lab	PL		-	-	3	50	50	100	1.5
							TOTAL	400	400	800	26

SEMESTER: V

Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1	14 EC 51	DIGITAL SIGNAL PROCESSING	PC		4			50	50	100	4
2	14 EC 52	ANALOG COMMUNICATION	PC		4			50	50	100	4
3	14 EC 53	MICROWAVE	PC		4			50	50	100	4
4	14 EC 54	VLSI	PC		4			50	50	100	4
5	14 EC E55X	Program elective-A	PE		4			50	50	100	4
6	14ECO56 X	OPEN ELECTIVE-B	OE		3			50	50	100	3
7	14 ECL57	DIGITAL SIGNAL PROCESSING LAB	PL		-	-	3	50	50	100	1.5
8	14 EC L58	LIC+AC LAB	PL		-	-	3	50	50	100	1.5
							TOTAL	400	400	800	26

SEMESTER: VI

Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1	14EC61	INFORMATION THEORY AND CODING	PC		4			50	50	100	4
2	14EC62	DIGITAL COMMUNICATION	PC		4			50	50	100	4
3	14 EC 63	ANTENNA AND WAVE PROPOGATION	PC		4			50	50	100	4
4	14EC64	OPERATION RESEARCH	HU		4			50	50	100	4
5	14ECE65 X	Program elective-C	PE		4			50	50	100	4
6	14ECO66 X	OPEN ELECTIVE-D	OE		3			50	50	100	3
7	14ECL67	VLSI LAB	PL		-	-	3	50	50	100	1.5
8	14ECL68	ADC LAB	PL		-	-	3	50	50	100	1.5
9	14ECP69	SEMINAR	PP		-	-	3	25@	-	25@	-
							TOTAL	400	400	800	26

@Marks carried to VIII sem.

SEMESTER: VII

Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1	14EC71	FIBER OPTIC COMMUNICATION	PC		4			50	50	100	4
2	14EC72	COMPUTER COMMUNICATION NETEORK	PC		4			50	50	100	4
3	14ECH73	ENTREPRENEURSHIP DEVELOPMENT, MANAGEMENT & IPR	HU		4			50	50	100	3
4	14EC74	POWER ELECTRONICS	CE		4			50	50	100	4
5	14EC75X	PROGRAM ELECTIVE-E	PE		4			50	50	100	4
6	14EC76X	OPEN ELECTIVE-F	OE		4			50	50	100	3
7	14ECL77	POWER ELECTRONICS LAB	PL		-	-	3	50	50	100	1.5
8	14ECL78	COMPUTER COMMUNICATION NETWORK LAB	PL		-	-	3	50	50	100	1.5
9	14ECP79	MAJOR PROJECT-PHASE 1	PP		-	-	3	25@	-	25@	-
							TOTAL	400	400	800	25

@Marks carried to VIII sem

SEMESTER: VIII

Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1	14EC81	WIRELESS COMMUNICATION	PC				3	50	50	100	4
2	14EC82X	PROGRAM ELECTIVE -G	PE		4			50	50	100	4
3	14ECP83	INTERNSHIP /SELF STUDY/MINOR PROJECT$	PP		-	-	15	50+50^	100	200	15
4		MAJOR PROJECT-FINAL SUMISSION & EVALUATION									
							TOTAL	200	200	400	23

^Marks carried from VI and VII sem to VIII sem.

$Internship of 4-6 weeks in an approved Industry/R&D organization/Reputed academic Institution during summer semester after IV or VI semester.

LIST OF ELECTIVES
(Vth-VIIth semester)

PROGRAM ELECTIVE

SL. NO.	SUBJECT CODE	SUBJECT NAME
1	14ECE551	Digital Image Processing
2	14ECE52	Computer architecture and organization
3	14ECE553	Data structures using C++
4	14ECE554	System verilog
5	14ECE555	Solid State devices

PROGRAM ELECTIVE-B

SL. NO.	SUBJECT CODE	SUBJECT NAME
1	14ECO561	MEMS
2	14ECO562	Automotive electronics
3	14ECO563	Random Process
4	14ECO564	Embedded system
5	14EC0565	

PROGRAM ELECTIVE-C

SL. NO.	SUBJECT CODE	SUBJECT NAME
1	14ECE651	DSP architecture
2	14ECE652	Multimedia communication
3	14ECE653	Analog mixed mode VLSI
4	14ECE654	Radar Engg
5	14ECE655	Testing and Verification

OPEN ELECTIVE-D

SL. NO.	SUBJECT CODE	SUBJECT NAME
1	14ECO661	Linear algebra
2	14ECO662	Auto SAR-I
3	14ECO663	ARM processor
4	14ECO664	RTOS
5	14ECO665	

PROGRAM ELECTIVE-E

SL. NO.	SUBJECT CODE	SUBJECT NAME
1	14ECE751	Satellite communication
2	14ECE752	Advanced Digital Communication

OPEN ELECTIVE-F

SL. NO.	SUBJECT CODE	SUBJECT NAME
1	14ECO761	Cryptography
2	14ECO762	AutoSar-II

3	14ECE753	Digital VLSI Design
4	14ECE754	RF electronics
5	14ECE755	ASIC Design

3	14ECO763	Adhoc wireless network
4	14ECO764	Nanoelectronics
5	14ECO765	

PROGRAM ELECTIVE-G

SL. NO.	SUBJECT CODE	SUBJECT NAME
1	14ECE821	SOC
2	14ECE822	Error control coding
3	14ECE823	Wireless mobile network
4	14ECE824	
5	14ECE825	

SL. NO.	BS. SC (BS)	ENGG. CORE (EC)	PROG. CORE (PC)	CORE. ELE (PE)	OPE. ELE (OE)	HUM (HU)	PROJ/INT /SEMINAR	
1	9.5	13.5						23
2	9.5	13.5				2		25
3	4	3	19					26
4	4		23					26
5			19	4	3			26
6			15	4	3	4		26
7			14	4	4	4		25
8				4			17	23
	27	30	90	16	10	10	17	200

Engg. Mathematics – III

Subject code: 14MAT31 **Branch: EC/EE**

No. of hrs/week: 4-1-0 **Exam Hrs: 03**

Total no. of hrs: 50 **Max marks: 100**

Objectives: To understand the periodic and harmonic phenomena and to be able to model them using Fourier series.

To understand the advantages, limitations and applications of different numerical techniques.

To understand the basics and applications of integral transforms

Expected outcomes:

- Students understand that any periodic function can be converted to harmonic using trigonometric series and also learn to trace different periodic functions.
- Students learn the importance of numerical methods, advantage and disadvantages of the same and also the limitations of various methods
- Importance of using transforms like Laplace, Fourier and Z transforms is learnt.

Unit – I

10 hours

Z- transforms : Definition, Standard Z transforms, Linearity property, Damping Rule, Shifting rule, multiplication by n, Initial and final value theorems, bivariate z transforms, region of convergence, Inverse by partial fractions method, convolution theorem. Solution of differenceequations. 23.1-23.9 23.12-23.14, 23.15(Type II), 23.16 (text book 1)

Unit-II

10 hours

Fourier series: Euler's formulae, Dirichlet's conditions for Fourier series expansion, change of interval, Even and odd function, half range series, complex form of Fourier series, Practical harmonic analysis.

Fourier Transforms: Definition, Complex Fourier transforms, Cosine and Sine transforms, Properties, Inverse Fourier transforms convolution theorem and Parseval's identity.

10.1,10.2, 10.3,10.5,10.6,10.7,10.10,10.11, 22.1, 22.2, 22.4, 22.5, 22.6, 22.7 (Text book 1)

Unit – III

8 hours

Laplace Transforms: Definition, Transforms of standard functions, Transforms of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$, Laplace transforms of derivatives and integrals, Laplace transforms of periodic functions, unit step function, Dirac delta function . Inverse Laplace transforms, convolution theorem, solutions of 1st and 2nd order ODE using Laplace transforms 21.1-21.15 (Text book 1)

Unit – IV

12 hours

Solution of transcendental equations- Secant method, Newton Raphson method

Finite differences – forward, backward, central,

Interpolation- Newton's forward and backward formulae, Newton's divided difference formulae and Lagrange's formula for unequal intervals and inverse interpolation by Lagrange's formula,

Evaluation of derivatives using Newton's forward and backward difference interpolation formulae

Numerical Integration - Trapezoidal, Simpson's $\frac{1}{3}$ and $\frac{3}{8}$ rule,

2.3,2.5, 3.3, 3.6,3.9.1, 3.10.1, 5.2, 5.4.1,5.4.2,5.4.3 (Text book 2)

Unit – V

10 hours

System of equations: Solution of system of equations by Gauss Siedel method, LU decomposition, Solution of Tridiagonal system

Numerical solution of ordinary differential equations: Taylor's series method, Runge-Kutta 4th order method, Milne's predictor corrector method 6.3.6, 6.3.8, 6.4, 7.2, 7.5, 7.6.2(Text book 2)

Text Book: 1. Higher Engg. mathematics by Dr. B S Grewal, 42nd Edition

2. Introductory methods of numerical analysis, by S S Sastry, PHI India.

Reference Book: 1. Advanced Engg. Mathematics by Erwin E Kreyszig, 8th edition, Wiley.
2. Numerical Methods by Jain , Iyengar and Jain, New Age, 6th edition, 2012

ANALOG ELECTRONIC CIRCUITS

Semester: III **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title: Analog electronic circuits	**Course Code:** 14EC32
L-T-P: 4-0-0	**Credits:** 04
Total Contact Hours: 45hrs	**Duration of SEE:** 3 hrs
SEE Marks: 100	**CIE Marks:** 50

PRE REQUISITES :

1. **Basic electronics**
2. **Basics of electrical engg**

CO1:- Acquire the basic knowledge of Analog Electronic devices such as diodes, MOSFET, BJT and its necessary circuitry details.

CO2:- Develop the ability to analyze and design analog electronic circuits using discrete components (BJTs,FETs)

CO3:- Analysis of amplifier circuits using small - signal equivalent circuits to determine gain input impedance and output impedance

CO4:- Method of calculating cutoff frequencies to determine the bandwidth and Design of power amplifiers

COURSE OUTCOME TO PROGRAMME OUTCOME MAPPING

PO	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**I**
CO1	S	S	S	S	S	M						M
CO2	S	S	S	S	S	M						M
CO3	S	S	S	S	S	M						M
CO4	S	S	S	S	S	M						M

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT 1

Diode circuits and its applications: Transition and diffusion capacitance of a diode , Reverse recovery time of diode , Load line analysis, Rectifiers with Capacitor filters, Non linear applications of diode(Clippers & Clampers).

Transistor Biasing: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Design operations, Transistor switching networks, and stability factor derivation for fixed bias configuration only

Text 1: **Ch 1: 1.10, 1.11. ch2: 2.1,2,2, 2.6, 2.7,2.8,2.9. Ch4: 4.1 to 4.6, 4.8, 4.9 4.11, 4.12**

Text 2: **Ch 20 : 20.7** **9hrs**

UNIT 1I

BJT AC Analysis: Amplification in AC domain, BJT transistor modeling, re model(CB,CE configuration),Hybrid equivalent model, Hybrid Π model, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration.(Derivation of Zi,Z0,Av,Ai for the configurations.)

BJT Frequency Response (Both Low Frequency and high Frequency): General frequency considerations, low frequency response-BJT amplifier, Miller effect capacitance, High frequency response of BJT amplifier

T**ext 1**: **Ch5: 5.1 to 5.4, 5.5 to 5.14 . Ch9: 9.4 ,9.6,9.8,9.9** **9Hrs**

UNIT III

General Amplifiers: Cascade connections, Cascode connections, Darlington connections.

Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits.Feedback concept, Feedback connections type : Voltage Series Feedback, Voltage Shunt Feedback, Current Series

Feedback, Current Shunt Feedback, Practical feedback circuits: Emitter Follower Using Voltage Series Feedback, Single Stage transistor amplifier with unbypassed RE for current series, Voltage Shunt Negative Feedback using OP-AMP.

Text 1: Ch 5: 5.19 ,5.20. Ch 14:14.1 to 14.3 9Hrs

UNIT IV

Power Amplifiers: Introduction, Definitions and amplifier types : series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Class C and Class D amplifier circuits.

Distortion in Amplifiers.Amplitude distortions and harmonic distortions

T**ext 1: Ch : 12 12.1 to12.8 Text 2: Ch: 16: 16.2 9Hrs**

UNIT V

Field Effect Transistors : Introduction ,Construction and characteristics of JFET , Transfer Characteristics.

FET Biasing: Fixed Bias configuration, Self Bias, Voltage divider Bias (common source configuration only)

FET Amplifiers: FET small signal model, Biasing of FET, Common source,Common drain common gate configurations

Ch 6 : 6.1,6.3. ch7: 7.1, 7.2, 7.3,7.4 Text 1: Ch 8:8.1to 8.7 9Hrs

TEXT BOOK

TEXT 1: Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory", PHI/Pearson Education, 9th Edition.

TEXT 2 : Jacob Millman & Christos C. Halkias, "Electronic Devices and Circuits", Tata -McGraw Hill, 1991

Reference Books:

1. David A. Bell, "Electronic Devices and Circuits", PHI, 4th Edition, 2004
2. Malvino,Albert Paul "Electronic Principles", 6th edition ,2000

DIGITAL ELECTRONICS

Semester: III **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title Digital Electronics	**Course Code:** 14EC33
L-T-P 4-0-0	**Credits:** 04

Total Contact Hours: 45hrs	**Duration of SEE:** 3 hrs
SEE Marks: 100	**CIE Marks:** 50

PRE-REQUISITES:

A Fundamental course on Physics and Basic Electronics

- Students will be able to Understand the fundamental principles behind the practical design methodologies and styles for Digital circuits.
- Students will get to know the different design techniques available for the simplification of Digital circuits.
- Students will learn to design combinational and sequential circuits to any given specifications.
- Ability to understand current applications, trends and new directions in Digital design

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S		S							S	
CO2	S	S		S							S	M
CO3		S		S							M	M
Co4		S				W					M	M

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT - I

Introduction to different logic families: Electrical characteristics of logic gates-logic levels, noise margins, fan-in, fan-out, propagation delay, transition time, power consumption and power delay product.TTL inverter and NAND gate -circuit description and operation. Text 1: Ch 2.8

Boolean algebra and Combinational Networks:Introduction to Boolean algebra and theorems, min-terms/max-terms, equation complementation, simplification and reduction of Boolean expressions using identities and theorems, SOP/POS forms, implementation using NAND/NOR gates, combinational circuits, don't care conditions, additional Boolean operations and gates.

Text 2: Ch 3. 3.1 to 3.9 9 hrs

UNIT – II

Simplification of Boolean expressions: Formulation of the simplification problem, prime implicants and irredundant disjoint expressions, prime implicants and irredundant conjunctive expressions, reduction techniques: K-Map, Quine Mc-clusky tabulation method. Five-variable and six-variable K-Maps. Variable Entered Map Techniques.

Text 2: Ch 4.1-4.8, 4.14 9 Hrs

UNIT III

Logic Design with MSI components and programmable logic devices: Binary adders and subtractors , BCD adders, magnitude comparators, encoders and decoders, multiplexers and de-multiplexers. Code Converters: BCD-to-Excess 3, Excess 3-to-BCD, BCD-to-Seven Segment Display.

Text2: Ch 5.1 to 5.10 Text1: Ch 3-3.4

UNIT – IV

Sequential Circuits Analysis and Design: Sequential circuit definitions, Latches, Flip-Flops: Master Slave Flip Flops, Edge triggered Flip Flops, RS, JK, D and T Flip-Flops, characteristics tables, sequential circuit analysis, analysis with JK flip flops, Flip-Flop excitation tables, design procedure.

Registers and Counters: Registers, shift registers, construction and operations of shift registers: SISO, SIPO, PIPO, PISO. Counters: ripple counters, synchronous counters, UP/DN counters, BCD Counters and ring counters. Application of counters and shift registers.

Text 1: Ch 4 and Ch 5

UNIT – V

Memory and Programmable Logic Devices: Memory and Programmable logic devices definitions, random access memory (RAM), RAM integrated Circuits, Array of RAM IC's, Programmable logic technologies, read only memory (ROM), Programmable Logic Array, Programmable Array Logic Devices.

Text 1: chap 6

Text Books:

1) M Morris Mano And Charles R kime,, "Logic and Computer design Fundmentals", Pearson Education ,3rd Edition ,2006.

2) Donald D Givone "Digital Principles and Design", Tata McGraw Hill Edition,2002

References:

1. Tocci,"Digital systems, Principles and Applications", PHI/Pearson Education,6th Edition,1997.

NETWORK ANALYSIS

Semester: III **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title :Network Analysis	**Course Code:** 14EC34
L-T-P: 4-1-0	**Credits:** 04
Total Contact Hours: 45hrs	**Duration of SEE:** 3 hrs
SEE Marks: 100	**CIE Marks:** 50

PREREQUISITES:

- MATHEMATICS-1
- MATHEMATICS-2

Course Outcomes

1) Students will be able to understand and solve the problems related to networks.

2) Students will be in a position to simplify the complex circuits using network theorems

3) Students will be able to analyze simple DC circuits and AC circuits and plot the steady state response

4) Students are able analyze the network concepts and can apply the same for real time application.

PO	a	b	c	d	e	f	g	h	i	j	k
CO1	S	S	M	S							M
CO2	S	S	M	S							M
CO3	S	S	M	S							M
CO4	S	S	S							M	

Teaching Methods

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT I

Basic circuit analysis concepts: Circuit components, Sources of electrical energy, Standard input signal, Kirchhoff's Laws, Source transformation, Mesh analysis, Node analysis, Network equations for RLC circuits.

Text1: Ch 1, Ch 2 9 Hrs

UNIT II

Graph Theory and Network equations: Graph of a network, Trees, Co-trees and Loops, Incidence Matrix, Cut-set Matrix, Tie-se Matrix and loop currents, Number of possible trees of a graph, Analysis of networks, Duality.**Text1: Ch 3** 9 Hrs

UNIT III

Laplace transform and it's applications: Laplace transformation, Basic theorems, gate function, impulse function, Laplace transform of periodic functions, Solution of linear differential equation, Solution of network problems.

Text1: Ch 5, Ch 6 9 Hrs

UNIT IV

Network Theorems: Superposition theorem, Reciprocity theorem, Thevenin's theorem, Norton's theorem, Millman's theorem, Maximum power transfer theorem.

Text1: Ch 7 9Hrs

UNIT V

Two port Network: Characterization of linear time invariant two port network, open circuit impedance parameter, short circuit admittance parameter, transmission parameter, inverse transmission parameter, hybrid parameter, inverse hybrid parameter, relationship between parameters, input and output impedance in terms of two-port parameters.

Text1: Ch 8, Ch 10 9 Hrs

Text books:

1. Van Valkenburg M. E. "Nework Analysis", Prentice Hall of India Pvt Ltd. 3rd Edition, 2002

Reference books:

1. D. Roy Choudhury, "Networks and Systems", New Age International Pvt Ltd Publishers (January 30, 2010)
2. Edminister, Mahamood Nahvi, "Electric Circuits", Schaum's outlines, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2000.
3. Franklin F. Kuo, "Network Analysis and Synthesis",. John Wiley and Sons 2nd Edition, 2002

SIGNALS AND SYSTEMS

Semester: IV **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title: Signals and systems	**Course Code:** 14EC44
L-T-P: 4-1-0	**Credits:** 04
Total Contact Hours: 45hrs	**Duration of SEE:** 3 hrs
SEE Marks: 100	**CIE Marks:** 50

Pre-Requisites :

Mathematics-I and Mathematics -II

COURSE OUTCOMES:

- Students learn basics of signals and operations on signals.
- Students will be able to get the idea about general signals and system properties, linear, time-invariant systems, convolution sum and convolution integral, time and frequency domain representation of linear signals and systems.
- Students will be able to determine the response of LTI system for all possible inputs
- Students learn the basic concepts on Discrete-time (DT) and continuous-time (CT) Fourier series and Fourier transforms and Z transforms

COURSE OUTCOME TO PROGRAMME OUTCOME MAPPING

PO	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**I**
CO1	S	M	M								W	
CO2	S		M						W			
CO3	S	M	M	S					S		W	
CO4	S	M	S	S	S						W	

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
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UNIT - I

Introduction: What is a signal and what is a system, overview of specific system, classification of signals, basic operations on signals, elementary signals, systems viewed as interconnection of operations, properties of systems .

Text1: Ch 1 **9hrs**

UNIT - II

Time domain representations for LTI systems: Introduction, convolution: Impulse response representation for LTI systems, properties of the Impulse response representation for LTI systems Differential and Difference equation representation for LTI systems, Block diagram representation.

Text1: Ch 2 **9hrs**

UNIT - III

Fourier representations for signals: Introduction, discrete time periodic signals: DTFS, continuous time periodic signals: CTFS, discrete time non-periodic signals: DTFT, continuous time non-periodic signals: CTFT, properties of Fourier representations

Text1: Ch3 **9hrs**

UNIT - IV

Applications of Fourier representation: Frequency response of LTI system, FT representation for periodic signals, convolution and modulation with mixed signal classes, FT representation for discrete time signals, sampling, reconstruction of continuous time signals from samples, discrete time processing of continuous time signals, FS representation for finite duration non-periodic signals, computational applications of DTFS, efficient algorithms for evaluating the DTFS.

Text1: Ch 4 **9hrs**

UNITV

Z-Transform: Development of the z-Transform, Properties of z-Transform, The inverse z-Transform, Solution of Difference equations with initial conditions, Relationship between z and Laplace Transform, the bilateral z-Transform

Analysis of signals and systems: Transfer functions, system stability, parallel, cascade and feedback connections, system responses to standard signals, pole zero diagrams and graphical calculation of frequency.

Text2:ch 11, Ch 12.12.1 to 12.6 **9hrs**

TEXT BOOKS:

1. Simon Haykin and Barry Van Veen, “Signals and Systems” John Wiley and Sons, Inc., 2002
2. Michael J. Roberts, “Signals and Systems - Analysis using transform methods and MATLAB”, Tata McGraw-Hill , 1st Edition, 2003.

REFERENCE BOOKS:

1. Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab, "Signals and Systems", Pearson Education Asia / PHI, 2nd edition, 2002.
2. H. P Hsu, R. Ranjan, "Scham's outlines of Signals and Systems", TMH, 2006.
3. B. P. Lathi, "Linear Systems and Signals", Oxford University Press, 2005

Microprocessor and Microcontroller

Semester: III **Year:** 2014-15

Department: *ELECTRONICS AND COMMUNICATION*	*Regular Course*
Course TitleMicroprocessor and Microcontroller	***Course Code*****:** 10EC36
L-T-P: 3-0-0	***Credits:*** 03
Total Contact Hours**:** 35hrs	***Duration of SEE*****:** 3 hrs
SEE Marks: 50	***CIE Marks*****:** 50

Pre-requisites:

Students are expected to have the following topical knowledge upon entering this course:

- Sufficient knowledge of various digital blocks like registers, flip flops, etc.
- Ability to write algorithms for a particular task.

Course Outcomes:

- Students will learn architecture of 8086 microprocessor and its applications.
- Students will be able to write assembly language programs for 8086 microprocessor.
- Students will learn to interface processor with peripherals

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Average of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

Course Outcome to Programme Outcome Mapping

PO	a	b	c	d	e	f	g	h	i	j	k
CO1										S	
CO2	M	S	S	M					M		
CO3		M	S	S	S						

UNIT –I

CISC and RISC Processor Architectures, Harvard and Von Neumann memory architectures.Introduction to 8086microprocessor : Architecture of 8086Microprocessor, pin description of 8086 microprocessor,Minimum and Maximum mode of operation of 8086 microprocessor, addressing modes in 8086 microprocessor. 8 hrs

TEXT 1: 1.2, 1.3, 1.8, 1.9, 2.2

UNIT –II

Assembler directives and Instruction set of 8086 microprocessor, Assembly language programming examples on data transfer and data conversions. 8 hrs

TEXT: 2.3, 2.4, 3.4

UNIT –III

Programming examples using string instructions, procedures, macros and DOS interrupt 21H function to read a character from keyboard with and without echo, display character and string on console.7hrs

TEXT: 3.4,4.8,4.10

UNIT –IV

Basic peripheral and their interfacing with 8086:8255 PPI device and modes of operation of 8255 and interfacing withkeyboard, ADC, DAC and stepper motor. 7 hrs

TEXT 1:5.4, 5.5, 5.6, 5.7, 5.8

UNIT –V

8051 Microcontroller: Introduction to 8051,Architecture of 8051 Microcontroller,Pin description of 8051 Microcontroller, Addressing modes of 8051,Comparison between Microprocessor and Microcontroller

5hrs

TEXT 2: 3.0, 3.1, 5.1, 1.1 Text 3 : 8.1

TEXT BOOKS:

1. **Advanced Microprocessor and Peripherals**-A.K Ray and K.M.Bhurchandi, Tata McGraw Hill.
2. **The 8051 Microcontroller,** Kenneth J Ayala, Thomson Delmar Learning., 2nd edition.
3. **The 8051 Microcontroller and Embedded Systems-using assembly and C**- Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D McKinlay, Prenitice Hall India,Pearson,2006

REFERENCE BOOKS:

1. **Microprocessor and Interfacing, programming & Hardware**-Douglas V Hall,2nd Edition, TataMcGraw Hill

2**. Microprocessor Architecture ,Programming and Applications with the 8085-** Ramesh S Gaonkar,4thedition,Penram International.

ANALOG ELECTRONICS LAB

Sub Code : 14ECL37 **IA Marks : 50**

Exam Hours : 03hrs

Exam Marks : 100

PREREQUISITES :Basic Electronics and Basic Electrical Engineering

Course Outcomes:

1. Students will be exposed to the usage of various electronic equipments to carry out the design experiments
2. Students will be able to understand the working and verify the different semiconductor devices.
3. Students will be able to understand the operation of the transistors, the concept of biasing, and amplifier topologies.
4. Students will be able to explore the operation of oscillators and opamps.

PO	a	b	c	d	e	f	g	h	i	j	k	L
CO1	M	M	S	S							M	M
CO2	M	S	M	S							S	M
CO3	M	M		S							S	M
CO4	M	M		S							S	M

Experiment List:

1. Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.
2. RC coupled Single stage BJT amplifier. Determination of the gain- frequency response, input and output impedances.
3. BJT-RC Phase shift Oscillator and BJT – Hartley or Colpitts Oscillators
4. Design of Clipping circuits using diodes

5. Positive clamping and Negative clamping.
6. Design of BJT Darlington Emitter follower and determination of the gain, input and output impedances.
7. Verification of Thevinin's Theorem and Maximum Power Transfer theorem for DC Circuits
8. Design of BJT -Crystal Oscillator for the given frequency.
9. Design of a FET Voltage series feedback amplifier and determine the gain, frequency response, input and output impedances.
10. Design of voltage doubler circuit.

Note: Students are made to learn Pspice circuit simulation tool in theory.

DIGITAL ELECTRONICS LAB

Sub Code: 14ECL38 **IA Marks: 30**

Hrs/ Week: 03 **Exam Hours: 03**

Exam Marks: 50

Prerequisites:

1. **Basic electronics**

Course Outcomes

- Students will be able to realize the simplified expressions using basic and universal gates.
- Students will be able to design combinational and sequential circuits for an application.
- Students will be able to analyze and design mini projects based on principles of digital electronics
- Students will be able to develop the ability to understand current applications, trends and new directions in Digital design

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S		S							M	M
CO2	S	S		S	W						M	M
CO3		S		S	M						M	M
CO4											S	S

NOTE: Use discrete components to test and verify the logic gates. Lab View can be used for designing the gates along with the above.

1. Realization of All gates using diodes and transistors.
2. Simplification, realization of Boolean expressions using logic gates/Universal gates.
3. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
4. Realization of parallel adder/Subtractors using 7483 chip
5. BCD to Excess-3 code conversion and vice versa.
6. Realization of Binary to Gray code conversion and vice versa
7. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
8. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
9. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
10. Realization of 3 bit counters as a sequential circuit and MOD – N
11. Counter design (7476, 7490, 74192, 74193).
12. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
13. Wiring and testing Ring counter/Johnson counter.

SYLLABUS FOR 4th SEMESTER

Engg. Mathematics – IV

Subject code: 14MAT41 **Branch: ECE/EEE**

No. of hrs/week: 4-1-0 **Exam Hrs: 03**

Total no. of hrs: 50 **Max marks: 100**

Objectives: To understand the basics, applications and importance of probability theory, random process, sampling, linear algebra with applications to computer science through definitions, theorems and problem solving.

Expected outcome:

Students understand concepts and applications of probability, distributions, random process and sampling.

Students understand essentials and applications of linear algebra.

Students will be able model using statistical tools like hypothesis testing

Unit – I

Probability – Random experiments, sample paces, event, axioms, addition and multiplication, conditional probability, independent events, Baye's theorem (Revision only)

Random variable, discrete probability distribution, continuous random variables, continuous probability distribution, cumulative density function, Expectation, variance.

Joint distribution- continuous and discrete, expectation, variance, standard deviation, covariance

Binomial, Poisson, Exponential, Normal, Hyper geometric relations, gamma distribution,

(2.1, 2.2, 2.4, 3.2,3.3,2.7,2.8,2.10,3.11,3.12, 4.1,4.4,4.7,4.8,4.13,1.16,4.18,4.19,4.20 Text book 1)

10 hours

Unit – II

Population and sample, sampling with and without replacement, sampling distribution of means, variance and proportion, sample variance. Unbiased estimate, reliability, confidence intervals for mean, variance and proportion, statistical hypothesis, testing of hypothesis, Type I and II errors, one tailed, two tailed tests, t - distribution, χ^2 – test, test for goodness of fit.

(5.1,5.2,5.4,5.5,5.6,5.7,5.8,5.9,5.11,6.1,6.2,6.3,6.47.1,7.2,7.3,7.4,7.5,7.7,7.9,7.10,7.15 Text book 2)

12 hours

Unit – III

Random process- definition, classification, pdf, cdf, mean, auto correlation, Stationary and Ergodic random process, Poisson process

Markov process- Definition, examples, TPM, n – step transitional probabilities, regular, ergodic matrices, stationary distribution, classification of states, Markov chain with absorbing states, periodic, transient and recurrent states. (8.1,8.2,8.3,8.6,9.1,9.2,9.3Text book 3)

10 hours

Unit - IV

Vector spaces- definition, examples, Linear combinations, subspaces, Row space of a matrix,linear dependence, basis and dimension, linear mapping, linear operator, matrix representation of linear operator, change of basis. 4.2,4.3,4.4,4.5,4.7,4.8,5.2,5.3,6.2,6.3 (Text Book 2)

8 hours

Unit – V

Polynomial of matrices, Characteristic polynomial, Cayley Hamilton theorem, diagonalization, Eigenvalues and eigen vectors, minimal polynomial, Triangular form, Jordan canonical form, cyclic subspaces, Orthogonal vectors and subspaces, Gram Schmidt Orthogonalisation process.

9.2,9.3,9.4,9.7,10.2,10.7,10.8,7.6,7.7 3 (Text Book 2) **10 hours**

Text Books:

1. Probability and statistics, by Murray R Spiegel, J Schiller, R Alu Srinivasan, Schaum's outline series, second edition

2. Linear Algebra by Lipschitz, Schaum's outline series, second edition

3. Probability and random process by Miller and Childers.

Reference Books:

1. Probability and stochastic processes by R D Yates, D J Goodman, Wiley, 2nd edition.2012

2. Linear algebra and its applications, Gilbert Strang, 4th edition

LINEAR INTEGRATED CIRCUITS

Semester: IV **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title: Linear Integrated Circuits	**Course Code:** 14EC42
L-T-P:4-0-0	**Credits:** 04
Total Contact Hours: 45Hours	**Duration of SEE:** 3 Hours
SEE Marks: 100	**CIE Marks:** 50

Pre-requisites:

- Basic electronics

- Analog electronic circuits

Course Outcomes:

- Students will understand the principles behind the practical design methodologies and styles for linear integrated circuits
- Students acquire knowledge of OPAMPs for particular applications and know how to calculate the values of components that must be connected externally.
- Students will be able to apply systematic design approach for application specific Linear integrated circuits.

PO	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**
CO1	M			S	M						M
CO2	S	M									
CO3		S			M						
CO4	S	S	S							M	

Teaching Methodology:

- Blackboard teaching
- Power Point presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class
- Regular updating of the op –amp related activities in the world.

Assessment Methods

- Two Surprise Tests, 10 Marks each. Average of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Course Project(Mini project)
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT-I

Introduction to operational amplifiers: Operational amplifier description, Basic operational amplifier circuit, OPAMP 741 IC, Voltage follower circuit, Non-inverting amplifier, Inverting amplifier.

Operational Amplifier parameters: Input and Output voltage, Common mode and supply rejection ratio, Offset voltages and currents, Input and output impedances, Slew rate and frequency limitations. OPAMP as DC.

Amplifiers: Basing OPAMP, Direct coupled voltage follower, Direct coupled non inverting amplifier, Direct coupled inverting amplifier, Summing amplifier, Difference amplifier.

Text1:Ch.1, Ch. 2, Ch. 3 **9Hrs**

UNIT-II

OPAMP as AC Amplifier: Capacitor coupled voltage follower, high Zin, Capacitor coupled voltage follower, Capacitor coupled non inverting amplifier, High Zin, Capacitor coupled Non- inverting amplifier, Capacitor coupled inverting amplifier, setting the upper cut off frequency, Capacitor coupled difference amplifier, Use of single polarity supply.

OPAMP's frequency response and compensation: OPAMP circuit stability, Frequency and phase response, Frequency compensating methods (Lead and Lag only)

Text1: Ch. 4, Ch. 5: 5.1-5.9. **9 Hrs**

UNIT- III

Miscellaneous OPAMP linear applications: Voltage sources, Current sources and current sinks, Current amplifiers, Instrumentation amplifier.

Signal generators: Triangular/rectangular wave generator, Wave form generator design, Phase shift oscillator, Wein bridge oscillator,

Text1: Ch. 6: 6.1- 6.4, 6.8, Ch. 7, Ch. 8, **Ch. 10: 10.1, 10.3, 10.5.** **9 Hrs**

UNIT-IV

OPAMP Applications: Basic OPAMP applications, V to I and I to V converter, Precision half wave rectifiers, Precision full wave rectifiers limiting circuits, Clamping circuits, Peak detectors, sample and hold circuit, OPAMP circuits using diodes, Log and antilog amplifier, Multiplier and divider, Differentiator, Integrator.

OPAMPnonlinear circuits: OPAMP in switching circuits, crossing detectors inverting Schmitt trigger circuit, Non-inverting Schmitt circuits, Astablemultivibrator, and Mono stable multivibrator.

Text1: Ch. 9.

Text2: Ch. 4:4.1 - 4.2, 4.5 - 4.11 **9 Hrs**

UNIT-V

Voltage regulators: Series OPAMP regulators, IC voltage regulators

Active filters: First order active low pass active filter, Second order low pass filter, First order high pass filter, Second order high pass filter, Band pass filter, Band stop filter.

555 Timer: Monstable and Astable operations, Schmitt Trigger.

PLL: Basic principles, Phase Detector/Comparator, VCO, Low Pass Filter, PLL Applications.

D to A and A to D converters: Basic DAC techniques, AD converters, Weighted resistor DAC, R-2R ladder DAC Problems, AD converter, Parallel comparator A/D converter, Successive approximation ADC.

Text2: Ch. 6. 6.2, 6.3, Ch. 7.7.1, 7.3, Ch. 8 (Excluding Applications),

Ch. 9,Ch. 10 **9 Hrs**

Text Books:

1. David A. Bell," Operational Amplifiers and Linear IC's", PHI, 2nd edition, 2004.
2. D. Roy Choudhury and Shail B. Jain "Linear Integrated Circuits", New Age International, 2nd edition, 2006.
3. Ramakant A. Gayakwad, "Op - Amps and Linear Integrated Circuits", PHI, 4th edition,1999.

References:

1. Allen Holberg : Analog and Mixed mode VLSI"
2. Robert. F. Coughlin and Fred.F.Driscoll," Operational amplifiers amd Linear Integrated Circuits", Pearson, 2006.

CONTROL SYSTEMS

Semester: IV **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title :Control systems	**Course Code:** 14EC43
L-T-P: 4-1-0	**Credits:** 04
Total Contact Hours: 45hrs	**Duration of SEE:** 3 hrs
SEE Marks: 100	**CIE Marks:** 50

PREREQUISITES

- Mathematics-1 and Mathematicis-2

Course Outcomes

- Students will be able to represent the mathematical model of a system and analyze its transfer function.
- Students will be able to analyze the stability of the system through different methods.
- Students will be able to study the overall performance of linear Systems
- Students are able to apply the concepts of control system to real time application

PO	a	b	c	d	e	f	g	h	i	j	k
CO1	M	M		S	M						M
CO2	M	M									M
CO3	M	S			M						
CO4	M	S	S							M	

Teaching Methodology

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT - I

Modeling of systems: The control system, Mathematical models of physical systems- Introduction, Differential equations of physical systems – Mechanical systems, Frictions, Translational systems, Rotational Systems, Electrical systems, Analogous systems.

UNIT – II

Block diagrams and signal flow graphs: Transfer function, Block diagram algebra, Signal Flow graphs.Text1: Ch 1.1.1, 9 Hrs

Time Response of feed back control systems: Standard test signals, Unit step response of first and second order systems, Time response specifications of second order systems, steady state error and error constants.

Text1: Ch 5. 5.1, 5.2, 5.3, 5.4, 5.5, 9 Hrs

UNIT – III

Stability analysis: Concept of stability, necessary conditions for Stability, Routh- stability criterion, Relative stability criterion

Root-Locus Techniques: Root locus concepts, Construction of root loci, Stability of System.

Text1: Ch. 6.6.1, 6.2, 6.4, 6.5, 6.6 Ch 7. 7.1, 7.2, 7.3 9 Hrs

UNIT - IV

Stability in the frequency domain: Mathematical preliminaries, Nyquist stability criterion concept. Text1: Ch 9. 9.1, 9.2, 9.3 9 Hrs

UNIT V

Frequency domain analysis: Bode Plots, All pass and minimum phase systems, Experimental determination of transfer function, Assessment of relative stability using Bode Plots.

Text1: Ch 1. 1.1, Ch 2. 2.1, 2.2, 2.4, 2.5, 2.6, Ch 8.8.1, 8.4, 8.5, 8.6 9 Hrs

Text Books:

1. J.Nagarath and MGopa1,"Control Systems Engineering", New Age International(p) Limited Publishers, 4th Edition, 2008

Reference Books:

1. K.Ogata,"Modem Control Engineering" Pearson .Education Asia I PHI, 4th Edition, 2002.
2. K.Channa Venkatesh and D. Ganesh Rao, "Control Systems", Sanguine Technical Publishers.
3. Chi-Tsong Chen, "Analog and Digital Control System Design Transfer-Function, State-Space, and Algebraic Methods", OUP, 2006,

FIELDS AND WAVES

Semester: IV **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title Field and Waves	**Course Code:** 10EC44
L-T-P: 4-1-0	**Credits:** 04
Total Contact Hours: 45hrs	**Duration of SEE:** 3 hrs
SEE Marks: 100	**CIE Marks:** 50

Prerequisites:

Vector algebra

Mathematics-I and II

Course Outcomes:

1) A basic understanding of electro -and magneto -statics sufficient to enable further study of advanced fields and waves topics.

2) Formulate potential problems within electrostatics, magnetostatics and stationary current distributions in linear, isotropic media. and also solve such problems in simple geometries using separation of variables and the method of images.

3) Define and derive expressions for the energy both for the electrostatic and magnetostatic fields, and derive Poynting theorem from Maxwells equations and interpret the same in terms of laws and theorems.

4) Describe and make calculations of plane electromagnetic waves in homogeneous media, including reflection of such waves in plane boundaries between homogenous media.

Teaching Methodology:

PO	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**
CO1	S	S									W	
CO2	S	S	S	M			W			M		
CO3	S	S	M	M							W	
CO4	S	S	M	M							W	

- Blackboard teaching

- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT I

Vector Analysis: Scalars & vectors, Vector Algebra, the Cartesian coordinate system, vector components & unit vectors, vector field, Dot product & cross product, circular coordinate system, cylindrical coordinate system, spherical coordinate system.

Coulomb's Law and Electric Field Intensity: The Experimental law of Coulomb, Electric Field Intensity, and Field due to continuous Volume charge distribution, Field of a line charge, field of a sheet charge.

Electric Flux density, Gauss's Law & Divergence: Electric Flux density, Gauss Law, Applications of Gauss' Law: Differential Volume Element, Divergence, Maxwell's First Equation (Electrostatics),The vector operator DEL and Divergence Theorem.

Text 1: Ch 1.1, 1.2,1.3,1.4,1.5,1.6,1.71.8,1.9, Ch 2.2.1 to 2.5, Ch 3.3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7

9 hrs

UNIT II

Energy and Potential: Energy & potential in a moving point charge in an Electric Field, The Line Integral, |Definition of potential difference & potential, The potential field of a point charge, The potential field of a system of charges: conservative property, Potential Gradient, The Dipole, Energy density in the Electric Field.

Conductors, Dielectrics and Potential: Current & current density, continuity of current, metallic conductors, conductor properties & boundary conditions. The method of images, Semiconductors, Nature of Dielectric materials, Boundary conditions for perfect dielectric materials, Capacitance, several capacitance examples, capacitance of a two wire line.

Poisson's and Laplace Equations: Poisson's & Laplace Equations, Uniqueness theorem, Examples of the solutions of Laplace's equation & Poisson's equation.

Text 1: Ch 4. 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, Ch 5. 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, Ch 7- 7.1, 7.2, 7.3, 7.4 **9Hrs**

UNIT III

The Steady Magnetic Field: Biot-Savart Law, Ampere's Circuital Law,Curl,Stokes' Theorem, Magnetic Flux & Magnetic Flux density, The Scalar & Vector magnetic potentials, Derivation of steady magnetic field Laws.

Magnetic Forces: Force on a moving charge, Force on a Differential current element, Force between differential Current elements, Force & Torque on a closed circuit.

Text 1: Ch 8. 8.1 , 8.2, 8.3, 8.4, 8.5, 8.6, Ch 9. 9.1, 9.2, 9.3, 9.4 9hrs

UNIT IV

Time- varying fields & Maxwell's Equations: Faraday's Law, Displacement current, Maxwell's equations in point form, Maxwell's equations in Integral form, The Retarded potentials.

Text-1: Ch 10. 10.1, 10.2, 10.3, 10.4, 10.5 9hrs

UNIT V

The Uniform Plane wave: Wave propagation in Free space, Wave propagation in Dielectrics, The Poynting vector & power considerations, Propagation in good conductors: Skin Effect, Wave polarization.

Plane waves at Boundaries: Reflection of uniform plane waves at normal Incidence, Standing wave ratio, Wave reflection from multiple interfaces, Plane wave propagation in general Directions. **Text-1: Ch 12. 12.1, 12.2, 12.3, 12.4, 12.5, Ch 13. 13.1, 13.2, 13.3, 13.4**

9hrs

Text Books:

1. William H Hayt Jr. and John A Buck,"Engineering Electromagnetics", Tata McGraw-Hill, 6th Edition 2001.

Reference Books:

1. John Kraus, "Electromagnetics with Applications", Tata Mc-Graw Hill, 5th Edition 1999.
2. Edward C. Jordan, "Electromagnetic waves & Radiating systems", Prentice –Hall of India / Pearson education, 2nd edition, 1968.

DIGITAL SYSTEM DESIGN USING VERILOG

Semester: IV **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course

Course Title :**Digital System Design using Verilog**	**Course Code:** 14EC45
L-T-P: 4-0-0	**Credits:** 04
Total Contact Hours: 45 hrs	**Duration of SEE:** 3 hrs
SEE Marks: 100	**CIE Marks:** 50

Prerequisites:

Digital electronics

Course Outcomes

- Students will understand the basic concepts of verilog HDL.
- Students will acquire the ability to apply HDL in modeling combinational and sequential circuits.
- Students will able to understand the basic architecture of FPGA.
- Students will develop expertise in use of EDA tools in digital circuit modeling and simulation.

Teaching

PO	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**
CO1	M	M		M							
CO2	M	S		S	M						
CO3					S					S	S
CO4					S					S	S

Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT-I

Introduction: Overview of Verilog HDL, History,Major capabilities and module description.

Language Elements: Identifiers, comments, format, compiler directives, value set, data types, parameters, operands, operators, kinds of expression.

Text 1:Ch 1,2,3,4 **9 Hrs**

UNIT-II

Gate level modeling and user defined primitives: The built in primitive gates, multiple input gates, multiple output gates, tristate gates, pull gates, MOS switches, bidirectional switches, gate delays, an array of instances, implicit nets, A simple example, two to four decoder, master slave flipflop, parity circuit, Defining a UDP, combinational UDP, sequential UDP, example.

Text 1: Ch 5, Ch 6 **9Hrs**

UNIT - III

Data Flow and behavioral modeling: Continuous assignment and example, net declaration assignment, delays, net delays, examples: Master slave flip flop, magnitude comparator, Procedural constructs, timing control, block statement, procedural assignment, conditional statement, case statement, loop statement, procedural continuous assignment,

Text 1: Ch 7, Ch 8 **9Hrs**

UNIT -IV

Structural Modeling and other topics: Module, ports, model instantiation, external ports, examples, tasks, functions, system task and system function, Generic shift registers, Gray counter, Decade counter, Parallel to Serial Converter.

Text 1: Ch 9, Ch10

Synchronous Sequential Circuits: Moore and Mealy Machines,-definition of state machines- state machines as sequence controller-design of state machines-state table-state assignment-Transition-excitation table-logic realization-design example Serial adder.

Text 2 **9 Hrs**

UNIT V

FPGA based systems: Introduction-basic concepts-Digital design with FPGAs-FPGA based system design.

FPGA Fabrics-FPGA Architectures-SRAM based FPGAs –chip i/o-circuit design of FPGA fabrics-Architecture of FPGA fabrics-SPARTAN III and above versions-FPGA connectors. **Text 3**

9hrs

Text Books:

1. J. Bhasker," A verilog HDL Primer" BS Publications ,2nd Edition.
2. Samir Palnitkar, "Verilog HDL-A Guide to digital design and synthesis", 2nd Edition, Pearson education. 2003
3. Wayne Wolf,"FPGA based system design",reprint 2005.Pearson education"Electronics communication Systems",McGraw Hill,4th Edition,1992.

Reference Books:

1. Stephen Brown, Zvonko Vransic," Fundamentals of digital logic with verilog Design", TMH 2nd Edition.
2. Nazeih M.Botros, "HDL Programming (VHDL & Verilog)", John Weily - India & Thomson Learning, 2006

MICROCONTROLLER

Semester: IV

Semester: IV **Year:** 2014-15

Department: *ELECTRONICS AND COMMUNICATION*	*Regular Course*
Course Title Microcontroller	***Course Code*****:** 10EC46
L-T-P: 4-0-0	***Credits:*** 04
Total Contact Hours**:** 45hrs	***Duration of SEE*****:** 3 hrs
SEE Marks: 50	***CIE Marks*****:** 50

PREREQUISITES:

Programming experience with C and assembly is strongly recommended

COURSE OUTCOME

- Students will learn hardware, software and architectural details of 8051 microcontroller.
- Students will learn to program 8051 in assembly language and C, compile, execute and embed the code in flash memory for standalone embedded system applications using Keil IDE

- Students will learn to interface 8051 with external devices like LCD, Keyboard, DC Motor, Stepper Motor, ADC and DAC.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING

PO	1	2	3	4	5	6	7	8	9	10	11	12
CO1		M	S	S								M
CO2			M	S	S		M				M	
CO3				S	S		M				M	S

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by conducting objective type quiz based on topics covered in the class.

UNIT-I

Microprocessor and Microcontroller: Introduction, Microprocessor and Microcontrollers, RISC & CISC CPU Architectures, Harvard and Von – Neumann CPU architecture.

The 8051 Architecture: Introduction, 8051 Microcontroller hardware, input / output pins, Ports and circuits, External Memory, Timers, Serial Communication and Interrupts.

Addressing Modes and Operations: Introduction, Addressing modes, External data moves, Code Memory data moves, PUSH and POP Instructions, Data Exchanges, Example Programs.

Text 2: Ch1. 1.0 to 1.1, Text 2: Ch3. 3.0 to 3.6, Text 2. Ch 5 **9Hrs**

UNIT-II

Logical and Arithmetic: Byte level logical operations, Bit level logical operations, Rotate and swap operations, Example Programs. Arithmetic operations: Flags, Incrementing and decrementing, addition, subtraction, multiplication and division, decimal arithmetic, Example Programs.

Jump and Call Instructions: The jump and call Program range, jumps, calls and subroutines. Example Problems.

Text2: Ch 6, Ch7, Ch 8 **9 Hrs**

UNIT -III

8051 Programming in C: Data types and time delays in 8051C, I/O programming, logic operations, data conversion programs, accessing code ROM space, data serialization.

Timer / Counter Programming in 8051: Programming 8051 Timers in C, Counter Programming timers 0 and 1 in 8051 C

Text 1: Ch 7, Ch 9 **9 Hrs**

UNIT IV

8051 Serial Communication: Basics of serial Communication, 8051 connections to RS 232, 8051 serial communication Programming, Programming the second serial port, Serial programming in C.

Interrupts Programming: 8051 Interrupts, Programming timer interrupts, programming external hardware interrupts, Programming the serial communication interrupts, Interrupts priority in the 8051/52, Interrupt programming in C *Text 1: Ch 10, Ch 11*

9Hrs

UNIT V

8051 Interfacing and Applications: Interfacing 8051 to LCD, keyboard parallel and serial ADC, DAC, stepper motor interfacing and DC motor interfacing. Programming in C.

Text 1: Ch 12, Ch 13, Ch 17 **9 Hrs**

Text Books:

1. Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay, "The 8051 Microcontroller and embedded systems – using assembly and C", Prentice Hall India, Pearson, 2006
2. Kenneth Ayala, "The 8051 Microcontroller", Thomson Delmar Learning, 3rd Edition

Reference Books:

1. Predko,"Programming and customizing the 8051 micro controller", Tata McGraw Hill
2. Frank Vahid & Tony Givargis, "Embedded System design", John Wiley, 2002.

Michael J. Pont, "Embedded C", Pearson Education, 2002.

MICRO CONTROLLER LAB

Semester: IV **Year:** 2014-15

Department: *ELECTRONICS AND COMMUNICATION*	*Regular Course*

Course Title Microprocessor	***Course Code*****:** 10ECL48
	Credits: 04
Total Contact Hours**:** 03hrs/week	***Duration of SEE*****:** 3 hrs
SEE Marks: 50	***CIE Marks*****:** 50

PREREQUISITES:

Programming experience with C and assembly is strongly recommended

Course Outcomes

- Students will be able to program a microcontroller system in assembly and C.
- Students will be able to interface the system to switches, keypad and displays, A/D and D/A converters.

PROGRAMMING

1. Programming in Assembly level code.

   a. Block Transfer with and with out overlapping.

   b. Exchange of data

   c. Arrange data in Ascending and Descending order

   d. To find the largest number in an array.

   e. To add two 16 bit and 8 bit numbers

   f. To subtract two 16 bit and 8 bit numbers

   g. To multiply two 16 bit and 8 bit numbers

   h. To find the square of two 8 bit numbers

   j. To find the cube of an 8 bit number

   k. To implement mod 16, mod 10 up and down counter.

   l. To logically AND, OR, XOR two 8 bit numbers.

2 .Write a program in ALP for Code conversion

   a. BCD – ASCII
   b. ASCII – Decimal

c. Decimal – ASCII
d. Hex – Decimal
e. Decimal – Hex

11. Write a program in ALP for generating delay using Timer.
12. Write a program in ALP for transmitting data using serial communication.
13. Write a program in ALP using call instruction.
14. Write a program in ALP using conditional and unconditional jump instructions.

INTERFACING

Programming in C language.

1. Implement simple calculator using 6 digit seven segment display and Hex Key board interface to 8051.
2. Alpha Numeric LCD panel and Hex keypad input interface to 8051.
3. External ADC and temperature control interface to 8051.
4. Generate different waveforms sine, square, triangular, ramp using DAC interface to 8051
5. Stepper and DC motor control interface to 8051.
6. Elevator interface to 8051.
7. Write code to generate different waveforms (Sine, Square, Triangle, Ramp, stair case etc.,) using DAC change the frequency and amplitude.

DSD using Verilog Lab

Semester: IV **Year:** 2014-15

Department: ELECTRONICS AND COMMUNICATION	Regular Course
Course Title DSD using verilog lab	**Course Code:** 10ECL47
Total Contact Hours: 03hrs/week	**Duration of SEE:** 3 hrs
SEE Marks: 50	**CIE Marks:** 50

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinfi/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PREREQUISITES:

Digital electronics

Course Outcomes

- Students will be able to design digital circuits using a Verilog language.
- Students will understand the implementation of digital systems by programmable devices, such as FPGA
- Students will able to use CAD tools to design and analyze digital systems.
- Students will be familiar with the synthesis of digital circuits.

CO-PO MAPPING

PO	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**l**
CO1	W	W		S	S							
CO2			S		S						M	
CO3				S	S						S	M
CO4				S	M							

PROGRAMMING (using VERILOG)

1. Realizing the logic gates using HDL.

2. Realizing the combinational designs using HDL

    a. 2 to 4 decoder

    b. 8 to 3 (encoder without priority & with priority)

    c. 8 to 1 multiplexer

    d. 4 bit binary to gray converter

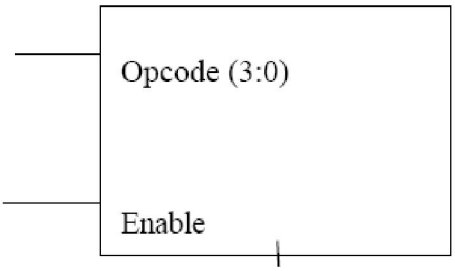
    e. Multiplexer, de-multiplexer, comparator.

3. HDL code to describe the functions of a Full Adder Using three

Modeling styles.

4. Model for 32 bit ALU using the schematic diagram shown below

A (31:0) B (31:0)



- ALU should use combinational logic to calculate an output based on the four bit op-code input.
- ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.
- ALU should decode the 4 bit op-code according to the given in example below.

OPCODE	ALU OPERATION
1.	A + B
2.	A – B
3.	A Complement
4.	A * B
5.	A AND B
6.	A OR B
7.	A NAND B
8.	A XOR B

5. Develop the following flip-flops, (SR, D, JK, T) using HDL

6. Design of 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and “any sequence” counters download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinfi/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

Interfacing programs

1. Implement a verilog code to control speed and direction of steeper motor
2. Write a verilog code to display 0 to F on a seven segment display