SYLLABUS

(2016-2017)

Master of Technology
In

VLSI DESIGN AND EMBEDDED SYSTEMS

NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY

Govindapur, Gollahalli, Yelahanka

Bangalore - 560064

PROGRAM OUTCOME

P01: Scholarship of Knowledge: The graduates will acquire in-depth knowledge and requisite skills in designing VLSI chips and embedded system and also will be able to develop new design methodology.

P02: Critical Thinking: The graduates will develop expertise in analyzing VLSI chips and embedded system requirement, convert it into design specification, develop advanced VLSI and embedded systems and also formulate standard for design, verification and testing methodologies.

P03: Problem Solving: The graduate will be able to analyze VLSI and embedded system requirement, formulate alternate design solutions and arrive at optimal solution considering cost, reliability, safety and environmental factors.

P04: Research Skill: The graduates will be able to perform literature survey , review research papers and reports, extract desired information, use CAD tools and also the advanced equipment required for design, verification and testing of VLSI chips and embedded systems.

P05: Usage of modern tools: The graduates will be able to use EDA tools, software and hardware to design, verify and test VLSI and embedded systems.

P06: Collaborative and Multidisciplinary work: The graduates will be able to work in large multidisciplinary design teams to achieve the goals of developing and integrating VLSI chips and embedded systems and also will be able to communicate with other team members sharing knowledge and expertise.

P07: Project Management and Finance: The graduate will be able to manage effectively the VLSI and embedded system design projects within given financial and time constraints and will also be able to integrate VLSI chip and embedded systems into a larger multidisciplinary project.

P08: Communication: The graduate will be able to write effective reports, make presentations, prepare design documentation as per the required Standards and communicate effectively with team members and stakeholders.

P09:Life-long Learning: The graduate will engage in life-long learning and upgrade their knowledge and skills in design, verification and testing of VLSI chips and embedded systems.

P10: Ethical Practices and Social Responsibility: The graduate will have professional and intellectual integrity and engage in design, verification and testing of VLSI chips and embedded systems considering sustainable development of society.

P11: Independent and Reflective Learning: The graduate will observe and examine critically the impact of one’s actions and make amends.

NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY, BANGALORE

SCHEME OF TEACHING AND EXAMINATION FOR

M.Tech. VLSI Design and Embedded Systems

SEMESTER: I

Sl.No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/Week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1.	16VES101	Advanced Mathematics	PC	ECE	4	0	0	50	50	100	4
2.	16VES102	CMOS VLSI Design	PC	ECE	4	0	2	50	50	100	5
3.	16VES103	Advanced Embedded System	PC	ECE	4	0	2	50	50	100	5
4.	16VES104	Digital System Design using Verilog	PC	ECE	4	0	2	50	50	100	5
5.	16VES105Ex	Program Elective–Group A	PE	ECE	4	0	0	50	50	100	4
6.	16VES106P	TERM PROJECT	PE	ECE	0	0	6	50	50	100	3
7.	16VES107S	SEMINAR	PC	ECE	0	0	4	50	50	100	2
TOTAL								**350**	**350**	**700**	**28**

PROGRAM ELECTIVE – GROUP A

Sl No	Subject Code	Subject Name
1	16VES105E1	VLSI Process Technology
2	16VES105E2	VLSI for Signal Processing
3	**16VES105E3**	**MEMS and NanoElectronics**

Note:

1. Department can swap the credits between the core and elective but make sure that the total credits for the semester remains same.
2. External examination should be combined for Seminar and Mini project (Viva Voce) but separate marks sheet should be submitted.

* Continuous Internal Evaluation ** Semester End Exam

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SCHEME OF TEACHING AND EXAMINATION FOR

M.Tech. VLSI Design and Embedded Systems

SEMESTER: II

Sl.No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/Week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1.	16VES201	Analog and Mixed mode VLSI Design	PC	ECE	4	0	2	50	50	100	5
2.	16VES202	Advance MicroController	PC	ECE	4	0	2	50	50	100	5
3.	16VES203	LINUX for Embedded systems	PC	ECE	4	0	2	50	50	100	5
4.	16VES204Ex	PROGRAM ELECTIVE – GROUP B	PC	ECE	4	0	0	50	50	100	4
5.	16VES205Ex	PROGRAM ELECTIVE – GROUP C	PE	ECE	4	0	0	50	50	100	4
6.	16VES206P	TERM PROJECT	PE	ECE	0	0	6	50	50	100	3
7.	16VES207S	SEMINAR	PE	ECE	0	0	4	50	50	100	2
TOTAL								**350**	**350**	**700**	**28**

PROGRAM ELECTIVE – GROUP B			PROGRAM ELECTIVE – GROUP C		
Sl.No	**Subject Code**	**Subject Name**	**Sl.No**	**Subject Code**	**Subject Name**
1.	16VES204E1	High Speed VLSI Design	1.	16VES205E1	Embedded System Testing
2.	**16VES204E2**	**Low Power VLSI Design**	2.	16VES205E2	System Engineering
3.	16VES204E3	ASIC Design	3.	16VES205E3	Automative ES
4.	16VES204E4	VLSI Verification using system Verilog	**4.**	**16VES205E4**	**Real time operating systems**

Note:

1. Department can swap the credits between the core and elective but make sure that the total credits for the semester remains same.
2. External examination should be combined for Seminar and Mini project (Viva Voce) but separate marks sheet should be submitted.

*Continuous Internal Evaluation ** Semester End Exams - Internal evaluation by the guide, # - External Examiner Evaluation (Thesis

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SCHEME OF TEACHING AND EXAMINATION FOR

M.Tech. VLSI Design and Embedded Systems

SEMESTER: III **CREDIT BASED**

Sl.No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/Week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1.	16VES301S	SEMINAR/FIELD WORK/PROFESSIONAL TRAINING/ SELF STUDY/TERM PAPER	PC	ECE	0	0	8	50	50	100	4
2.	16VES302P	PROJECT PHASE -1	PC	ECE	0	0	32	50	50	100	16
							Total	**100**	**100**	**200**	**20**

Note:

1. External examination should be combined for SEMINAR/FIELD WORK/PROFESSIONAL TRAINING/ SELF STUDY/TERM PAPER and PROJECT PHASE -1 (Viva Voce) but separate marks sheet should be submitted.

2. The Project willcommence immediately after the II semester.

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SCHEME OF TEACHING AND EXAMINATION FOR

M.Tech. VLSI Design and Embedded Systems

SEMESTER: IV

Sl.No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/Week			Examination			Credits
					L#	T#	P#	CIE*	SEE**	Total	
1.	16VES401P	PROJECT PHASE -2- THESIS ASSESMENT*	PC	ECE	0	0	15	100$	100#	200	08
2.	16VES402P	PROJECT PHASE -2- INTERNAL EVALUATION AND VIVO VOCE$	PC	ECE	0	0	24	100	100	200	16
							TOTAL	**200**	**200**	**400**	**24**

Note:

1. PROJECT PHASE -2- THESIS ASSESMENT* : The evaluation under this title involves two components
    a. Thesis evaluation by the external examiner will be considered as SEE
    b. Thesis evaluation by the internal examiner will be considered as CIE
2. PROJECT PHASE -2- INTERNAL EVALUATION AND VIVO VOCE$: The evaluation under this title involves two components:
    a. Final Viva Voce jointly conducted by the Internal and External examiner will be considered as SEE
    b. Continuous evaluation of the project throughout the semester by a committee(at departmental level) will be considered as CIE.

* Continuous Internal Evaluation ** Semester End Exam

$ - Internal evaluation by the guide, # - External Examiner Evaluation (Thesis)